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INTERNATIONAL EDITION
OCTOBER 30, 1986

EDN

Accelerator boards upgrade PC performance

Low-cost devices handle S/D, R/D conversion

Data compression for bit-mapped displays

Electronica '86

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Batteries furnish backup power for sensitive data and circuits

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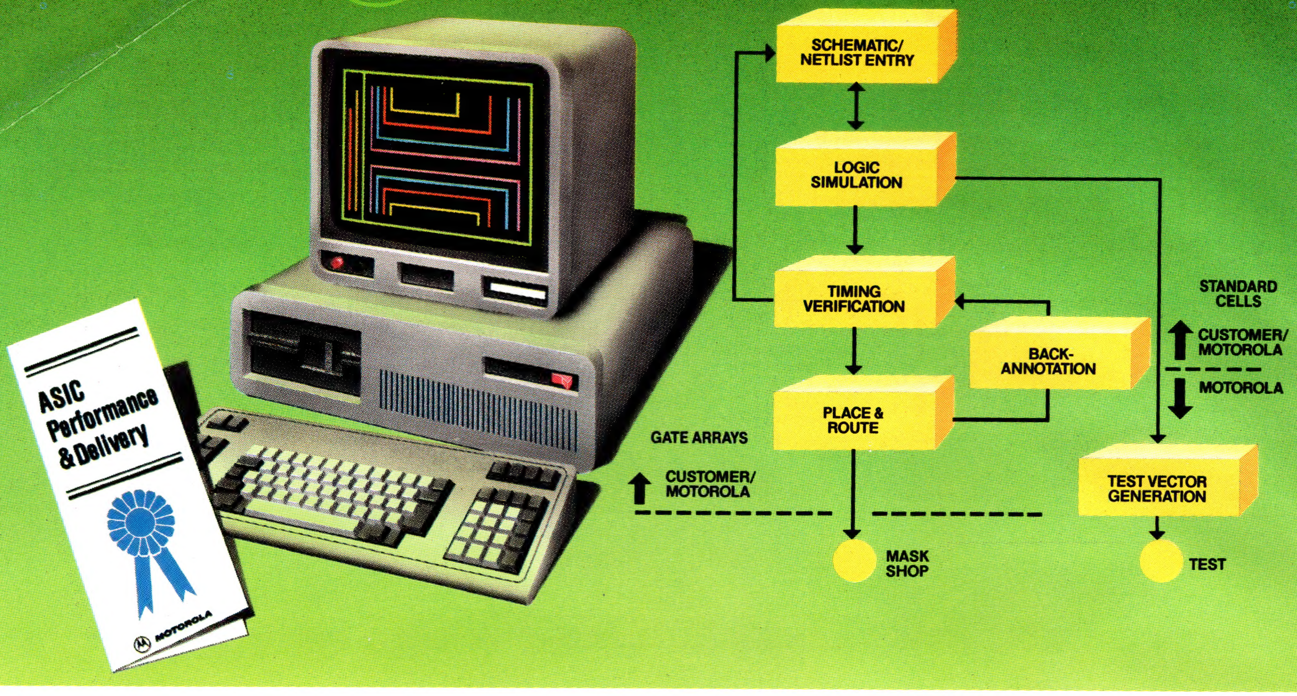

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Circle 84 for Literature Only

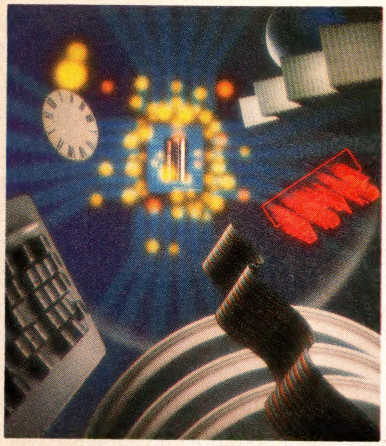
Circle 123 for Direct Factory Response

Volume 31, Number 22

EDN

October 30, 1986

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



***On the cover:** Manufacturers are offering batteries in a variety of package styles and in chemistries that range from alkaline to zinc. You can choose models that provide backup power for a small portion of critical circuitry or for complete systems. See pg 132. (Photo courtesy Eveready)*

DESIGN FEATURES

Special Report: Backup batteries 132

Battery makers are making steady improvements in both the chemistry and the mechanical construction of batteries. As a result, design engineers now have such a plethora of battery types to choose from that they can match virtually any application, to an appropriate battery system.—*Charles H Small, Associate Editor*

Single-port MAC speeds 68000 matrix products 155

A single-port multiplier/accumulator IC overcomes speed constraints placed on system performance by the long multiplication times of μPs. Compared with add-on bit-slice multiplication accelerators, the device offers an easier and more economical solution to multiplication needs in digital-signal-processing applications.—*David Fair, Analog Devices Inc*

Compressing data conserves memory in bit-mapped displays 173

Most bit-mapped information is highly redundant and therefore transmitting and storing every pixel is a waste of time and memory. You can save storage space and speed data-transmission rates in bit-mapped workstations by using a chip that employs standard CCITT algorithms to compress data.—*Peter M Fuchs, Advanced Micro Devices*

Programming schemes change applications role of EPROMs 191

Fast programming algorithms, gang programmers, and device-handling equipment allow OEMs to maximize EPROM-programming yields while still getting end products to market quickly.
—*Denise Slocombe, Data I/O Corp*

Continued on page 7

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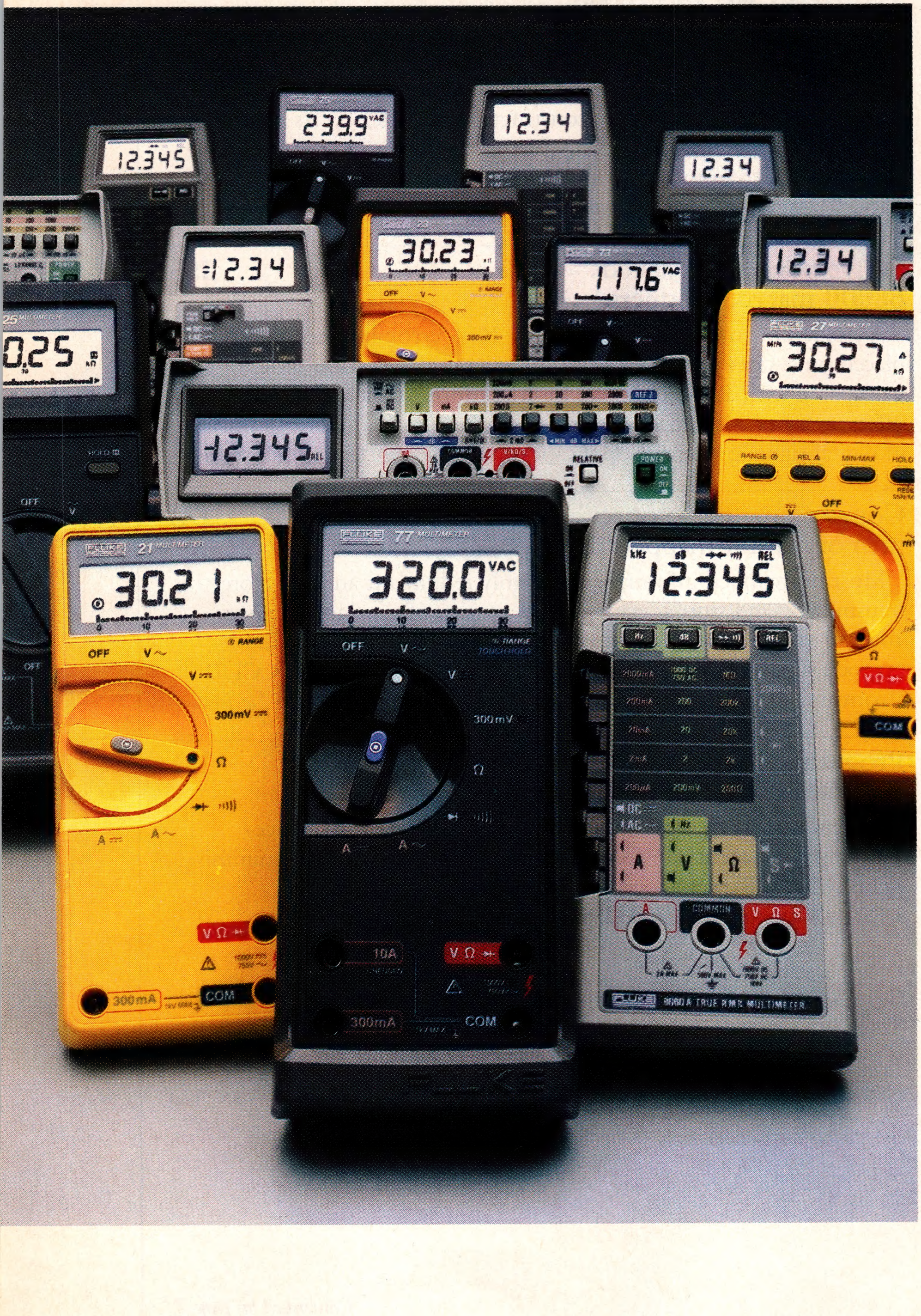

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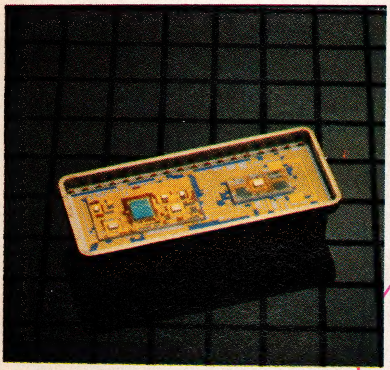

***Hybrid converters** are finding use in a variety of motion-control systems that employ synchros or resolvers (pg 61).*

TECHNOLOGY UPDATE

Synchro/resolver converters bring low cost and small size to motion-control systems 61

Modular and hybrid converter microcircuits are making the synchro/resolver (S/R) approach to angle measurement increasingly attractive.*—Tarlton Fleming, Associate Editor*

Accelerator boards boost speed of PCs and achieve performance comparable to PC/ATs 73

If your budget won't allow you to buy a PC/AT, but your applications require the speed that a PC/AT offers, you can speed up your PC or PC/XT by installing one of the many accelerator boards currently available for as little as $100 to $995.*—Chris Terry, Associate Editor*

Electronica 86 conferences cover topics from VLSI devices to power semiconductors 87

Electronica 86, which takes place November 11 to 15 in Munich, West Germany, provides not only an opportunity to survey new product offerings in the electronic-component and -assemblies market, but also an opportunity to attend four technical conferences.
—Peter Harold, European Editor

Wescon/86 will highlight CAE applications and high-speed analog and digital ICs 103

Engineers who attend Wescon/86 will have the opportunity to view the latest electronic-product innovations and get tips on their applications and design criteria.*—Margery S Conner, Regional Editor*

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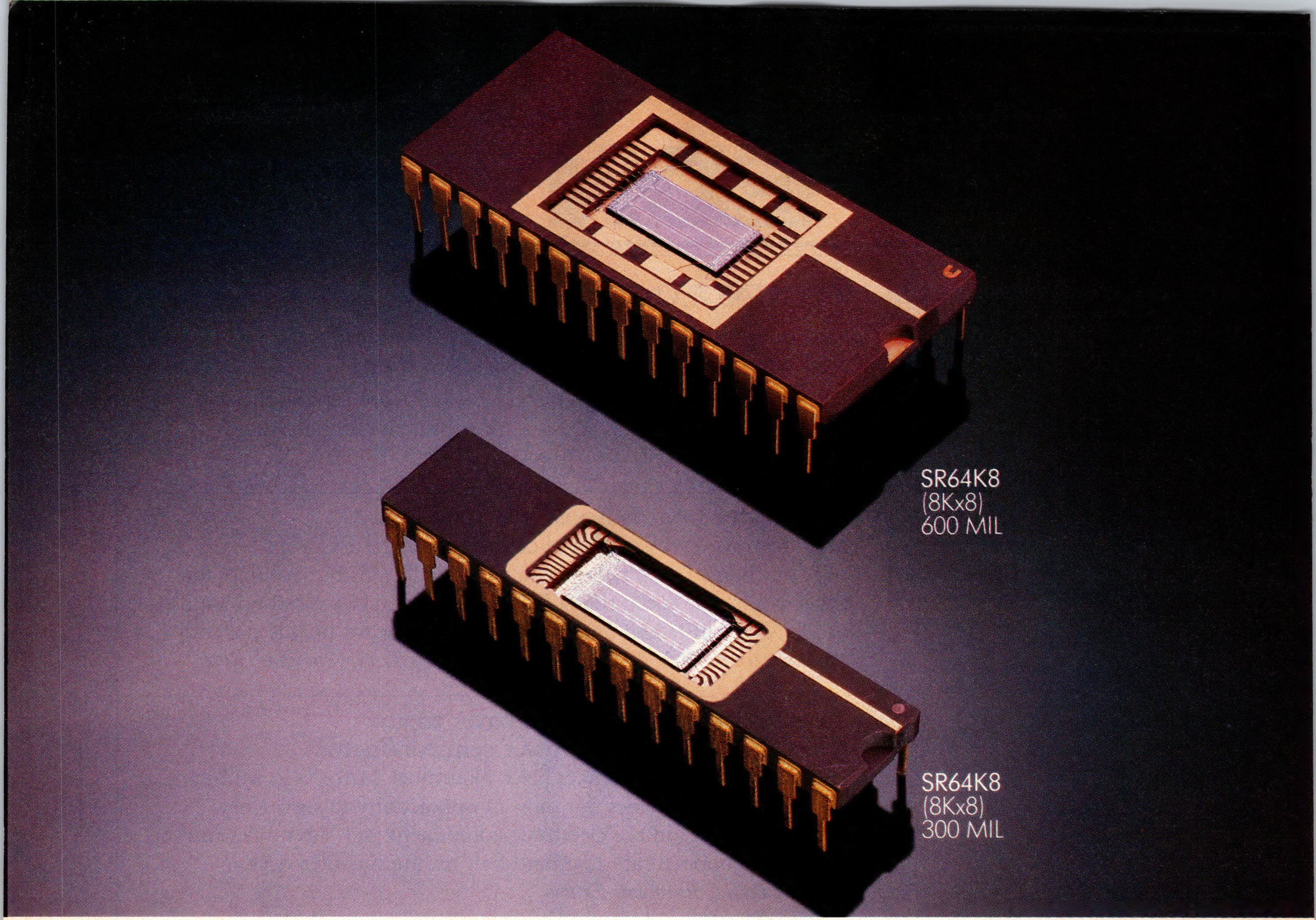

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Opportunities outweigh perils of the market for engineers at fledgling workstation maker.—*Deborah Asbrand, Staff Editor*

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Multilayer types lead growth in market for pc boards.

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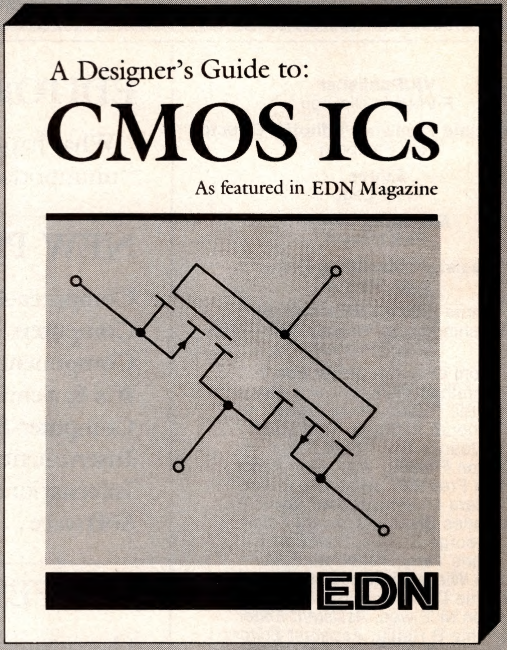

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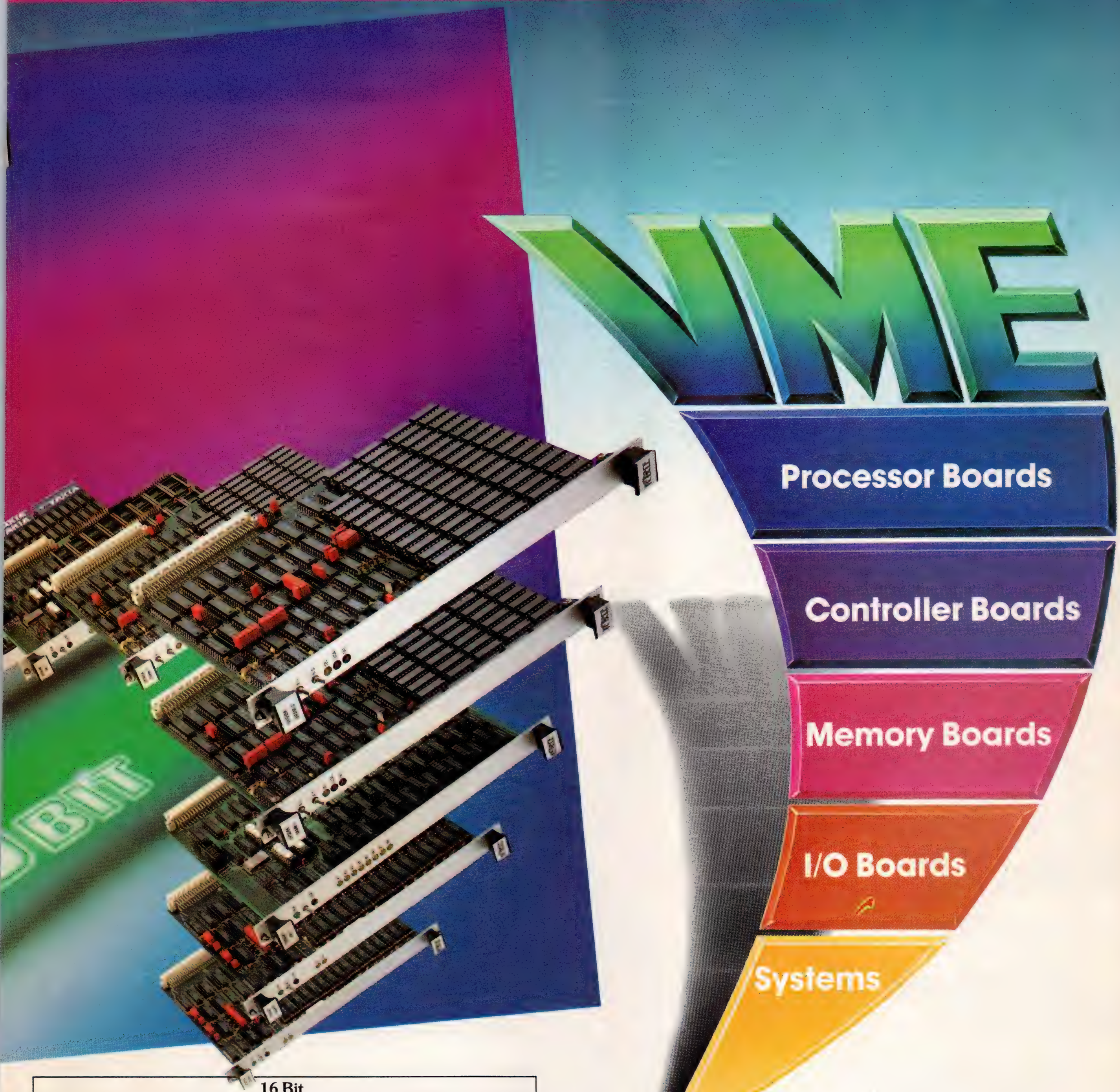

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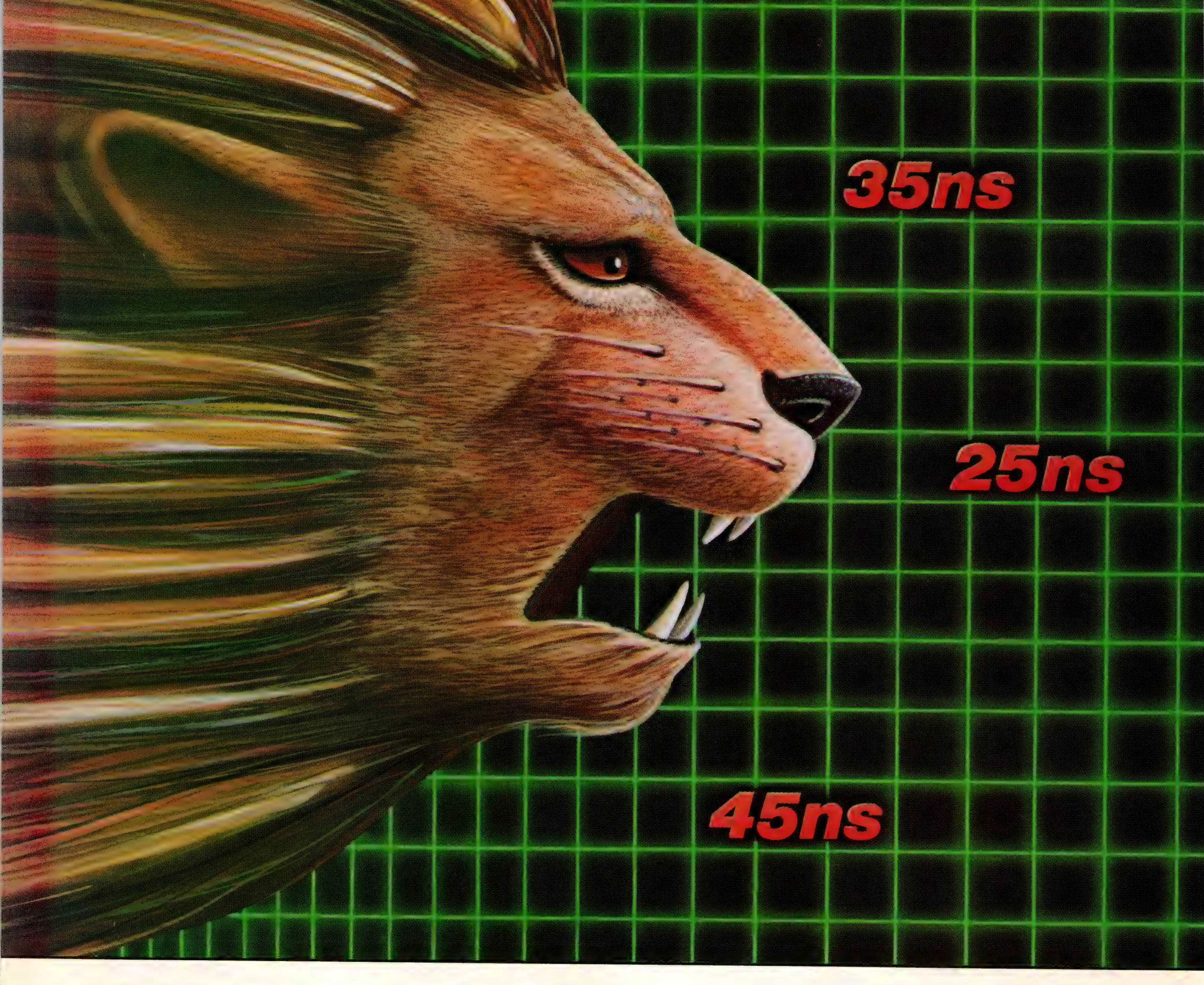

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For high speed bit-wide applications, we are in full production of two versions of our CMOS 64K x 1 SRAMs. One with access times to 45ns, and one with the lowest standby power in the industry at only 100μA.

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For additional byte-wide applications, we are introducing an 8K x 8 device with access times to 35ns. Packaging is standard 28 pin 600 mil plastic dip. For applications where parity is required, we have an 8K x 9 with speeds to 35ns in a 28 pin 300 mil ceramic dip.

So when you're thinking fast, think Toshiba, the power — and the speed — in static RAMs. Toshiba. The Power in High Speed RAMs.

FAMILY TYPE: HIGH SPEED MOS STATIC RAMS

PART	ORG'N	SPEED	PACKAGE		SAMPLES	PROD'N
TMM2068D	4KX4	55	20P	CDIP	NOW	NOW
TMM2068D	4KX4	45	20P	CDIP	NOW	NOW
TMM2068D	4KX4	35	20P	CDIP	NOW	NOW
TMM2068AD	4KX4	25	20P	CDIP	9/86	11/86
TMM2078D	4KX4	55	22P	CDIP	NOW	NOW
TMM2078D	4KX4	45	22P	CDIP	NOW	NOW
TMM2078D	4KX4	35	22P	CDIP	NOW	NOW
TMM2078AD	4KX4	25	22P	CDIP	9/86	11/86
TMM2018D	2KX8	55	24P	CDIP	NOW	NOW
TMM2018D	2KX8	45	24P	CDIP	NOW	NOW
TMM2018D	2KX8	35	24P	CDIP	NOW	NOW
TMM2018AD	2KX8	25	24P	CDIP	12/86	12/86
TMM2089C	8KX9	45	28P	SBDIP	NOW	10/86
TMM2089C	8KX9	35	28P	SBDIP	NOW	10/86
TMM2088P	8KX8	45	28P	DIP	9/86	12/86
TMM2088P	8KX8	35	28P	DIP	9/86	12/86
TC55416P	16KX4	45	22P	DIP	11/86	2/87
TC55416P	16KX4	35	22P	DIP	11/86	2/87
TC55416P	16KX4	25	22P	DIP	UNDER DEVELOPMENT	
TC55417P	16KX4	45	24P	DIP	11/86	2/87
TC55417P	16KX4	35	24P	DIP	11/86	2/87
TC55417P	16KX4	25	24P	DIP	UNDER DEVELOPMENT	
TC5561P	64KX1	70	22P	DIP	NOW	NOW
TC5561P	64KX1	55	22P	DIP	NOW	NOW
TC5562P	64KX1	55	22P	DIP	NOW	NOW
TC5562P	64KX1	45	22P	DIP	NOW	NOW

NOTE: DIP = PLASTIC CDIP = CERDIP SBDIP = SIDE BRAZED CERAMIC

TOSHIBA.
THE POWER IN HIGH SPEED SRAMS.

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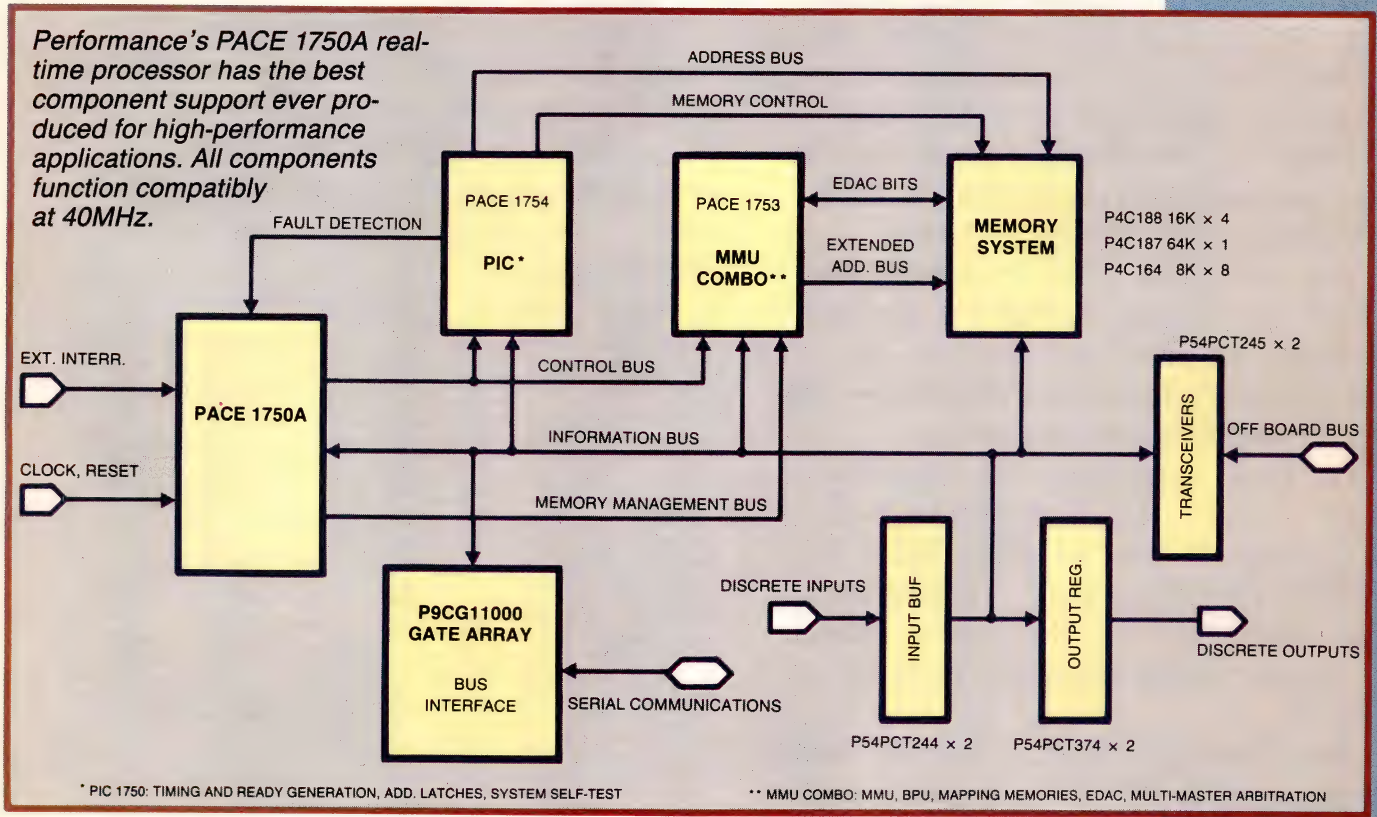
CIRCLE NO 181

WORLD'S FASTEST CMOS REAL-TIME CPU

5 MIPS
40 MHz



Performance's PACE 1750A real-time processor has the best component support ever produced for high-performance applications. All components function compatibly at 40MHz.

* PIC 1750: TIMING AND READY GENERATION, ADD. LATCHES, SYSTEM SELF-TEST

** MMU COMBO: MMU, BPU, MAPPING MEMORIES, EDAC, MULTI-MASTER ARBITRATION

- **CMOS *single-chip 1750A military standard* for 16 bit—20, 30, or 40MHz**
- **5 MIPS integer processing at 40MHz**
- **32-bit and 48-bit floating point**
- **2.6 MIPS at 40MHz for DAIS floating point instruction mix**
- **Less than 1 watt at 40MHz**
- **−55°C to +125°C**
- **Complete component support includes three ultra-fast 64K SRAMs: 16Kx4, 64Kx1, and 8Kx8 (over full military temperature), bus interface octals, Memory Management Unit, Processor Interface Circuit, and gate arrays with 11,000 gates for any remaining customizing functions.**

EDN103086

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THE MAKING OF A BREAKTHROUGH

1750A. 40MHz. Single-chip CMOS implementation of the military standard. Pretty impressive specs, and no small feat. Why did we do it? Because we knew you needed it. How did we do it? The unusual way. We planned and managed for early success.

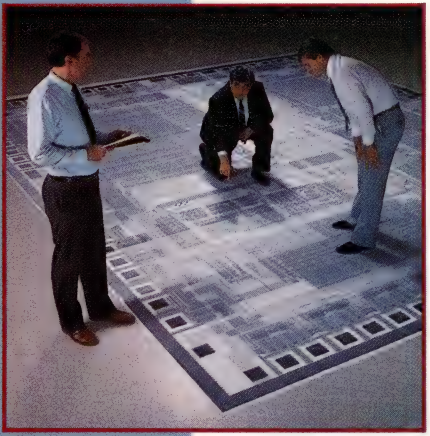
We started by creating a fresh new conceptual architecture and logic design; it improved the chip's performance by a factor of 2.

We put the chip through its paces against the 1750A instruction set in exhaustive ATP tests.

We pushed our advanced CAE tools to the limit, and debugged them designing Performance static RAMs and logic circuits. Then we put the tools to work on the 1750A.

Our Class-2 facility produces 6-inch wafers with 0.8 micron CMOS technology.

Thousands of man days later, we achieved a complete chip layout verification on the computer against the circuit schematic. An impressive feat in itself.



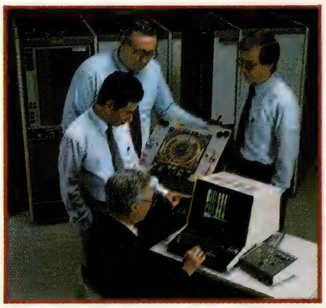
Performance engineering put 200,000 transistors in just 52,000 square mils.

PACE TECHNOLOGY

As a designer, you know that you can't create advanced products without advanced manufacturing methods. That's why our process people built a Class-2 facility to process 6-inch wafers, and developed PACE Technology, the most advanced CMOS technology available today: 0.8 micron effective channel lengths, 2.75 micron metal pitch, and internal loaded gate delays of 500 picoseconds. PACE Technology made it possible to achieve a 40MHz clock rate on the 1750A.

We debugged PACE Technology on a 400,000 transistor 64K SRAM, a good test prior to processing the 200,000 transistor PACE 1750A.

But advanced technology alone cannot assure success. That's why we depended on the ideas and skills of our managers. Our top fifteen managers each have an average of over fifteen years of semiconductor industry experience.



It was gratifying to watch 1750A chips from the very first wafers pass Sentry test.

The payoff? *Working chips in the first wafers of our first pass of silicon.*

The 1750A passed the full 100,000 vector test program, over the full military temperature range, 5 volts ± 10%.

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SEMICONDUCTOR CORPORATION

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Dedicated to your future.

INTERFERENCE SUPPRESSORS
General Technical Information

The tests described below are those among the tests which are significant for capacitors used as interference suppressors for which national approvals are required.

Standard	Test voltage in type test	Endurance test at +85 (100)°C 1000 h
SEN 432901 (IEC 161)		
X-application	1075 VDC 1 min	1.5 × U_R
Y-application	1500 VAC 1 min	1.7 × U_R
EMKO 1(N, D, EI)		
X-application	1075 VDC 1 min	1.5 × U_R + 1000 V, 50 Hz 0.1 sec each hour*
Y-application	1500 VAC 1 min	1.7 × U_R + 1000 V, 50 Hz 0.1 sec each hour*
SEV		
X-application	1075 VDC 1 min 3 kV surge**	1.5 × U_R
Y-application	1500 VAC 1 min 5 kV surge**	1.7 × U_R
VDE 0565-1		
X-application	1075 VDC 1 min (X_1, X_2) 4 kV surge (X1)**	1.25 × U_R + 1000 V, 50 Hz 0.1 sec each hour*
Y-application	1500 VAC 1 min	1.7 × U_R + 1000 V, 50 Hz 0.1 sec each hour*
IEC 65	2000 V 50 Hz 1 min Surge: 50 discharges from 1 nF capacitor charged to 10 kV	500 V 50 Hz + 100 V 50 Hz 0.1 sec each hour 1500 hours*
UL 1414 Across-the-line	120 V, 60 Hz + 5 kV surge 50 discharges from 1 nF capacitor charged to 10 kV	220 or 440 VAC 0.1 sec ea 220
Antenna coupling and line-by-pass		

* figure 1
** figure 2

186

INTERFERENCE SUPPRESSORS
General Technical Information

Figure 1. Endurance test
According to IEC 384-14 the capacitor shall be connected to a 220 Ω resistor during the 1000 V period

During an IEC-65 test no resistor shall be used.

During 1985 some countries will make decisions of not using any resistor.

Figure 2. Surge voltage test
According to SEV:
Up for X cap = 3 kV
Up for Y cap = 5 kV
According to VDE and IEC 384-14:
Up for X1 cap = 4 kV

Figure 3 Charge/discharge test.
According to VDE 0565/1 the capacitors shall be tested 10000 pulses at 100 V/us and √2 × U.. for PHE 800 and PHE 810.

RIFA tests the capacitors with metallized paper as dielectric 10 times the specified values in the article tables. 10000 pulses and X capacitors 630 VDC. IEC 65 and Y capacitors 1000 VDC

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CIRCLE NO 190

HOW TO GET THE RIGHT ARRAY RIGHT AWAY.

THE RIGH

Building a semicustom logic system is far more complex than it has to be.

First, you have to go from one manufacturer to another to find all the parts you need. Then you have to go to some out-of-the-way facility to create your design. And when that's finally done, you still have to wait — and wait — for finished production.

Wouldn't it be easier if you could get all your semicustom logic and all your design software from one source, design everything on your own workstation, and be sure of getting finished parts in quantity and on time?

Well now you can. And in the next seven pages, we'll tell you how.

MLA GATE ARRAYS. A HIGHLY INTEGRATED FAMILY.

Whatever you're looking for in semicustom logic, you've come to the right page.

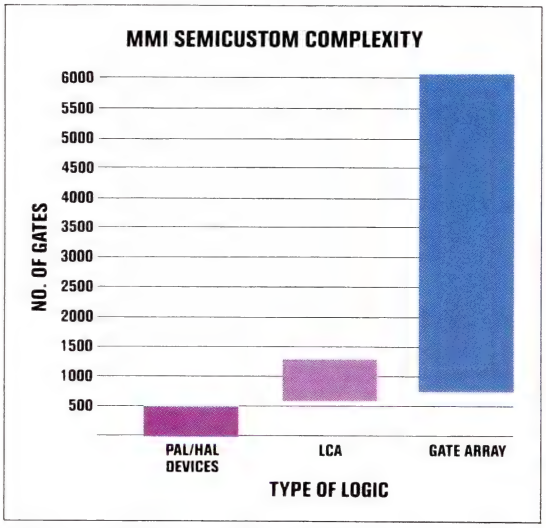
If it's higher integration, for instance, our new MLA family of CMOS gate arrays has just what you need. There are eight part types in all. With density ranges of 700 to 6000 gates. The fastest internal speeds around, with gate delays of less than 1 ns and flip-flops that run at over 150 MHz. The highest drive output available, at 16 mA per output, worst case. And a guaranteed gate utilization of 85%.

THE PROGRAMMABLE LOGIC CELL ARRAY.™ THE BEST OF BOTH WORLDS.

Maybe you'd rather have something a lot like a gate array, but in a lot less time. Then look at our new field-programmable M2064 Logic Cell Array.™ It gives you real gate array density, with up to 1200 usable gates, plus the speed to keep pace with system clock rates of up to 50 MHz.

The LCA™ architecture is highly flexible, and made up of three elements: Logic Blocks, I/O Blocks and Interconnect. All logic functions and interconnections are determined by memory cells, so the part is never physically altered. Instead, it's electronically programmed. And can be reprogrammed as often as you like.

It also offers all the benefits of full user programmability. Such as instant prototyping. Off-the-shelf availability. And no NRE charges.



Whatever your complexity needs, Monolithic Memories has the solution.

PAL DEVICES. TRUE FEATS OF LOGIC.

Our PAL® devices give you the same advantages of user programmability, and a broader range of design options. And we offer a range of architectures and speed/power options you won't find anywhere else. If you're looking for speed, try our 6 ns ECL circuits, or our new 10 ns TTL PAL20D parts. And if you want low power, see our new CMOS ZPAL™ circuits. With zero standby power, they're the industry's first "true" CMOS PAL devices.

For random logic applications or state machine design, consider our PAL20RA10, with 10 user-configurable input/output macrocells and independent clocks, or our new PAL32VX10, a pin-compatible superset of the 22V10, offering the added benefits of buried registers and reconfigurable flip-flops.

ARRAYS.

WRITE

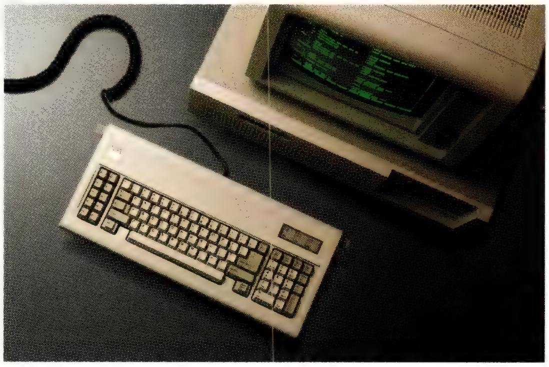
Once you've decided which type of logic to use, the rest is simple.

Because all three types — gate array, LCA and PAL devices — can be designed on your own PC-based workstation. With our easy-to-use software supporting you all the way.

HOW TO GATE ARRAY.

Even first-time gate array users will find our design software and documentation to be comprehensive and easy to use.

They allow you to do your complete design right on your own workstation. With the confidence that you'll receive prototypes in four weeks. Prototypes that will work in your system the first time.



Our easy to use design software lets you build any type of logic on your own IBM® XT- or AT-based workstation.

Our menu-driven software takes you through the whole design process in a natural progression of steps, resulting in a high-integrity design for your system and all the information we need to produce a working part. You get on-line help and documentation. Automatic simulation compare programs. The ability to create your own datasheet. A comprehensive check and quality control program. Over 200 characterized macrocells. And the option of designing with Boolean Equations.

You also get truly comprehensive documentation, including split page format, graphic examples and a self-paced tutorial approach that will have you designing in no time at all.

Best of all, you'll avoid the time, trouble and expense of designing on a mainframe in some out-of-the-way development site.

We've established a system to allow you to design at your facility and be supported by a fully-staffed network of local service centers. Each offers feasibility evaluation, training and design system access. As well as design Q.C. and acceptance, layout and post-layout verification of your design.

HOW TO LCA.

Designing an LCA is as easy as ABC.

Our design software allows schematic capture with standard programmable logic block primitives, which can be configured with either Karnaugh Map or Boolean Equations. What's more, it allows verification of internal timing. Logic and AC simulation. In-circuit emulation. And more.

And, because the LCA is reconfigurable, you can program it one day, and reprogram it the next.

You can also get extra design support from our local FAE offices. Each is equipped with a full development system for one-on-one training.

HOW TO PAL.

This shouldn't take long at all. Because our PALASM® 2 CAD software lets you configure any PAL device quickly, easily and effectively.

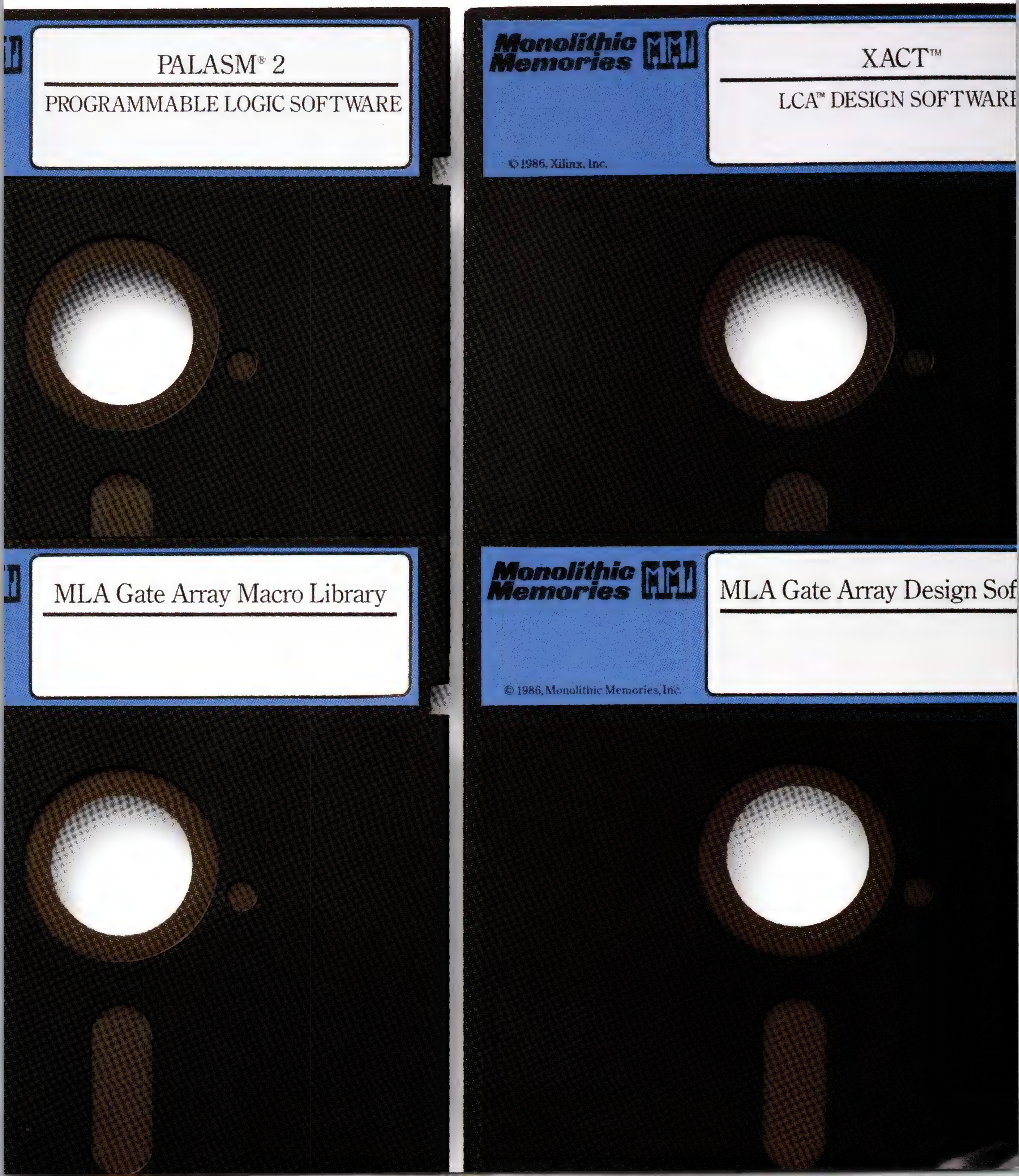
You can create your design file with Boolean or State Equations. You can simulate your design before your device is programmed. You can even reduce your logic equations automatically. And, if you need any extra help, you can get free, unlimited support from the experts at our FAE offices.

HIGHER INTEGRATION. WITHOUT FRUSTRATION.

Suppose you want to convert your PAL-based design into a more highly integrated gate array. No problem. Our PAL Device Integrator™ software lets you do it automatically. Without the time, trouble and expense of re-designing.

The PAL Device Integrator converts previously designed PALASM 2 equations to an equivalent gate array model consisting of specially-designed macrocells that can be simulated and easily merged with the rest of your design. It also outputs a schematic of the converted equations that can be viewed or modified through the schematic capture editor.

AWAY.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RIGHT

Monolithic Memories has virtually eliminated the most frustrating aspect of building complex logic.

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Because the moment your design is completed, we're ready to bring it to production. In the quantity you want. And in precisely the time you want it.

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Our dedicated gate array manufacturing facilities are optimized for turnaround. And, unlike most other facilities, they're designed to handle both large and small orders. In single or multi-wafer volumes.

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Best of all, our gate array production lines are already up and running. We're shipping finished circuits to customers. And cutting weeks off their time to market.

YOUR PART IN A MAJOR PRODUCTION.

You can also send your LCA and PAL device prototypes to us (or to our distributors) for volume production. We're both equipped to provide cost-effective, low-risk manufacturing, in quantity and on time.

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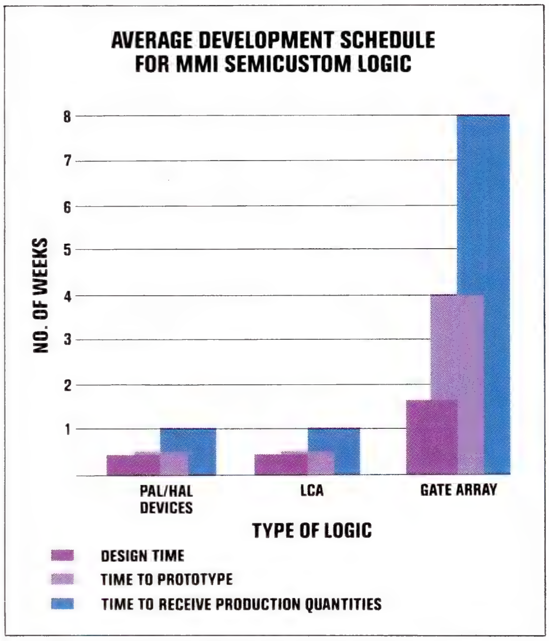

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NEWS BREAKS

EDITED BY JOAN MORROW

LOGIC ANALYZER FEATURES 100-pSEC TIMING RESOLUTION

The T-100 logic timing analyzer from Outlook Technology (Campbell, CA, (408) 374-2990) offers three unusual measurement techniques in addition to its 350-MHz synchronous data-acquisition mode. In the first mode, you can direct the analyzer to synchronously sample data at a harmonic of the external clock. Consequently, you can have as many as 16 synchronized data samples per external clock period instead of just one. With the second synchronous detection mode, you can offset the analyzer's sampling clock in 100-psec increments from the external mode and make your synchronous measurements. In the third mode the analyzer will take a synchronous measurement, automatically offset its sampling clock a fixed amount of time from the external clock, take a second measurement, and continuously repeat the process until it can compile a composite recording with data points displayed every 100 psec.

Using an IBM PC/XT host, you can configure the analyzer's 32 channels for data acquisition (to 2 GHz in asynchronous mode) or pattern generation or both. The pattern generator operates to 250 MHz with each channel's pattern independently programmable to 4k bits in length. The T-100, Outlook Technology's first product, will be available in January for $27,500 to $40,000.—Chris Everett

VME BOARD PROVIDES LOW-COST ETHERNET NODE CONTROL

If you need an inexpensive Ethernet node controller for VME Bus workstations, consider the $1295 V/Ethernet 3207 from Interphase Corp (Dallas, TX, (214) 350-9000). This double-height card contains 256k bytes of dual-ported data-buffer RAM and supports slave data transfers, slave control/status transfers, seven levels of programmable interrupts, and serial interfaces for Ethernet and Cheapernet. The 3207 uses AMD's 7990 Lance chip and features a software-configurable ring-buffer architecture with separate receive and transmit buffers.—J D Mosley

CMOS 1M-BIT STATIC-RAM MODULE FITS IN 32-PIN DIP

Although 1M-bit monolithic static RAMs may be a year or more off, you can specify a hybrid equivalent today. For example, Dense-Pac Microsystems (Garden Grove, CA, (714) 898-0007) offers the Model DPS 41288 1M-bit static-RAM module. Organized as 128k bytes, it fits the JEDEC-standard 32-pin DIP package for 1M-bit static RAMs. You can choose military versions as well as modules with access times ranging from 70 to 150 nsec. The module carries four 32k-byte static-RAM ICs and one decoder. A 150-nsec, 0 to 70°C version costs $295 (100).—Maury Wright

KIT CUSTOMIZES SOCKETS FOR PGA PROTOTYPING

Using the Textool socket kit from 3M (Austin, TX, (512) 834-6563), you can build custom sockets for testing and prototyping unique pin-grid-array (PGA) IC packages. You can order these PGA socket kits in matrix sizes ranging from 10×10 to 21×21 pins. Each kit includes a baseplate, a cam lever that locks the socket contacts into position, assembly screws, and instructions. A zero-insertion-pressure feature protects fragile pins from damage during insertion and withdrawal. A 10×10 kit with 20 contacts and pattern plugs costs $14.95 (10).—J D Mosley

PLUG-IN BOARD ACCELERATES PC-BOARD AUTOROUTING

An option to Calay Systems Inc's (Irvine, CA) V04 pc-board layout system, the RPR-7, speeds up automatic routing. A reduced-instruction-set computer enables the plug-in board to route pc-board layouts as much as three times faster than the V04. The accelerator automatically routes layouts seven times faster than the company's V03 system. Furthermore, the system can route almost all pc-board layouts completely. The routing accelerator provides parallel access to grid memory and parallel execution of grid-cell mapping functions. The $19,500 system includes a 2M-byte, 2-port memory. You can extend the memory to as much as 16M bytes.—Eva Freeman

GRAPHICS BOARD COMPLETES ZOOMS AND PANS IN LESS THAN 2 SEC

If your primary complaint about PC CAD software is that it runs too slowly for effective use with complex vector drawings, consider the Nth Engine from Nth Graphics (Austin, TX, (512) 832-1944). When installed in your IBM PC or compatible computer, this board lets you complete zooms and pans in less than two seconds on drawings that take eight minutes on an IBM PC/AT with an EGA controller. Using an onboard 1M-byte vector-display list, an additional 2½ screens of raster display memory, and two graphics processors, the Nth Engine offers a sustainable data-transfer rate of 5M bytes/sec. A board offering 640×480-pixel resolution costs $2995; a 1024×768-pixel version costs $3995.—J D Mosley

HARDWARE ACCELERATES LOGIC AND FAULT SIMULATION

Three companies—Aida Corp (Santa Clara, CA), XCAT Inc (Hopkins, MN), and Zycad Corp (St Paul, MN)—have introduced hardware accelerators for logic and fault simulation. The packages are targeted for ASIC designers.

Aida's CoSim II can model as many as 1 million gates at a speed of 5 million evaluations per second. Before this system simulates a design, it calculates the order in which a stimulus vector passes through each gate in the design. Once the package has created a model of the design, it propagates signals through a circuit faster than an event-driven logic simulator can. The simulation accelerator, which you must connect to an Apollo workstation, costs $85,000.

The MXT-25 from XCAT simulates as many as 16,000 modeling elements at a speed of 2 million events per second. The vendor estimates that this speed is comparable to that of a 1000-MIPS computer. The hardware accelerator costs $39,000.

Prices for one of Zycad's Magnum accelerators start at $38,000; you can also lease one of these systems for $570 per month. The four members of this series of logic and fault accelerators can model 16,383 to 65,535 elements. The systems execute 25 to 100 MIPS.—Eva Freeman

PERIPHERAL CONTROLLER IC SHRINKS SINGLE-BOARD COMPUTER

The FE3010 peripheral controller IC from Faraday Electronics (Sunnyvale, CA, (408) 749-1900) replaces 21 discrete components on a PC/AT-compatible single-board computer (SBC), resulting in a space savings of 80% and a power savings of 70%. You can combine it with Faraday's FE3000 CPU controller IC to implement an SBC in two chips. However, the chip is not limited to 16-bit bus support; it will also support 80386-based systems.

The IC is compatible with 6-, 8-, and 10-MHz clock speeds and can accommodate 256k- and 1M-bit static RAMs. It incorporates 15 interrupt channels, a real-time clock/calendar, three timer channels, seven DMA channels, a page register, and refresh address logic. Fabricated in HCMOS 2-μm technology, the part is packaged in an 84-pin J-leaded surface-mount plastic chip carrier. Sample quantities are available now for $55 (100); production quantities will be available in December.—Margery S Conner

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TRW LSI Products Division, the industry leader in high performance digital signal processing products, gives designers an edge with the TDC1011. The TDC1011 is a high-speed, 8-bit wide shift register, programmable to any length between 3 and 18 stages. It operates at an 18MHz shift rate (56ns worst case), is TTL compatible, and dissipates a low 750mW.† The TDC1011 operates from a single +5V power supply and is available in a 24-lead DIP.

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NEWS BREAKS: INTERNATIONAL

BY PETER HAROLD

HIGHLIGHTS OF ELECTRONICA 86

EDN's primary coverage of new products on display at Electronica 86 in Munich, West Germany (November 11 to 15) begins on page 87, but here's a brief look at some last-minute entries.

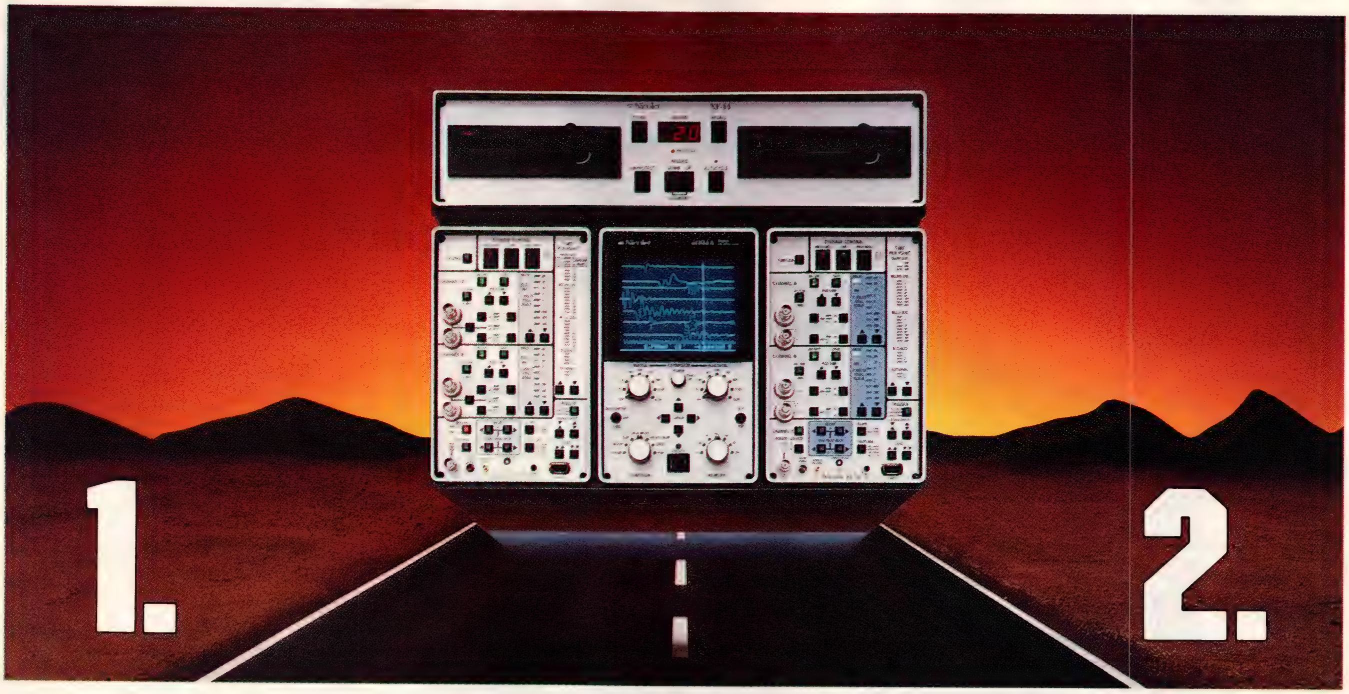
The MK5030 and MK5035 CMOS ICs from Thomson Components-Mostek Corp (Paris, France, TLX 240780 or Carrollton, TX, (214) 466-6000) will be shown in Hall 24, Stand 24-B-10. The devices allow you to implement Starlan—a 1M-bps local-area network (IEEE-802) that uses standard twisted-pair telephone wiring. Priced at less than $50 (OEM qty), the MK5030 Starlan hub chip controls as many as 12 radial LAN links and conforms to all IEEE-802.3 requirements. In addition, it automatically compensates for polarity reversals in the telephone wiring and provides status outputs to indicate network activity and faults on individual network links. Priced at less than $10 (OEM qty), the MK5035 encoder/decoder interfaces a variety of media-access-control chips to the Starlan network. It automatically compensates for polarity reversal of the network wiring and includes the multipoint extension and station-disconnect functions required in enhanced Starlan networks.

At Hall 24, Stand 24-B-4, Philips/Valvo (Eindhoven, The Netherlands, TLX 51573) will exhibit solid-state, frame-transfer image sensors, which provide compatibility with all major TV standards. The NXA1011 CCIR-compatible image sensor and the NXA1031 EIA-compatible sensor are monochrome devices suiting black-and-white camera applications. However, their high sensitivity at the blue end of the visible spectrum also suits them for use in 3-chip ENG (electronic news gathering) color cameras. For single-chip color applications, the NXA1021 and the NXA1041 have on-chip color-stripe filters. The NXA1021 provides an output compatible with pal or SECAM TV standards; the NXA1041 provides NTSC standard output. The image sensors have a 7.5-mm-diagonal imaging area, matching the format of a ½-in. camera tube. Scheduled for volume production in '87, the sensors will sell for $150 and $200 (OEM qty).

At Hall 20, Stand 20-D-26, Ashling Microsystems (Limerick, Ireland, TLX 70182) will display the CT64180 and CT80515 development systems. Operating in conjunction with an IBM PC, PC/XT, PC/AT or compatible computer, they provide program development, in-circuit emulation, and logic-state-analysis facilities for 64180 μP- and 80515 μC-based designs. Symbolic debugging is maintained through all stages of design, even when setting the trigger conditions for the logic analyzer. The CT64180 assembler supports directives to manage the μP's memory-management unit, and it assembles as many as 3000 lpm on a PC/AT to speed iterations around the design loop. You can set as many as 64k real-time breakpoints throughout the 512k-byte addressing range of the 68140 μP and detect when the μP has entered a low-power standby mode. The CT80515 development system is similar to the CT64180, and it supports all the 80515 μC ports including the A/D converter. Prices are approximately Sw fr 20,000 for the CT64180 and Sw fr 17,900 for the CT80515.

Operating on the G96 bus, the GESMPU-20 CPU card from Gespac (Geneva/Plan-les-Ouates, Switzerland, TLX 429989) will be on display at Hall 18, Stand 18-D-10. It includes a 12- or 16-MHz 68020 μP, 256k or 512k bytes of CMOS RAM, and space for 512k bytes of EPROM. The processor has zero-wait-state access to onboard memory. The board has five interrupt lines, which operate in either a vectored or autovectored mode, and can address as much as 32M bytes of memory with a 1-MHz (optionally 2-MHz) synchronous access cycle. You can order it with a 68881 math coprocesssor. A 12-MHz version with 256k bytes of RAM costs Sw fr 1700 (50).

THE FIRST NAME IN DIGITAL SCOPES



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bent lead version
style x 65

NSN GUIDE

MCL NO.	NSN
T1-1	5950-01-128-3745
T2-1	5950-01-106-1218
T4-1	5950-01-024-7626
TMO4-1	5950-01-067-1012
TMO4-2	5950-01-091-3553
T9-1	5950-01-105-8153
TMO9-1A	5950-01-098-6315
T16-1	5950-01-094-7439

case styles

T, TH, case W 38, X65 **Bent Lead Version**
TMO, case A 11, † case B13
FT, FTB, case H 16

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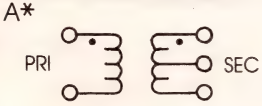
case style number see opposite page.		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Ea.	PRICE $ Qty.
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	3.95	(10-49)
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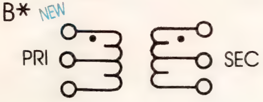
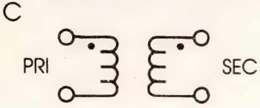
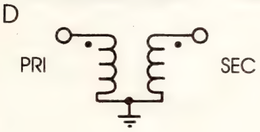
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.25	(10-49)
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	4.25	(10-49)
		T3-1T	3	.05-250	.05-250	.1-200	.5-70	3.95	(10-49)
		T4-1	4	.2-350	.2-350	.35-300	2-100	2.95	(10-49)
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	3.95	(10-49)
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.25	(10-49)
		T8-1T	8	.03-140	.03-140	.10-90	1-60	6.95	(10-49)
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.25	(10-49)
		T16-6T NEW	16	.03-75	.03-75	.06-30	.1-20	4.95	(10-49)
	TH	T4-1H	4	8-350	8-350	15-300	25-200	4.95	(10-49)
	TMO	TMO1-1T	1	.05-200	.05-200	.08-150	.2-80	6.45	(10-49)
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	6.75	(10-49)
		† TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	6.75	(10-49)
		† TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	6.45	(10-49)
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	4.95	(10-49)
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	6.75	(10-49)
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	6.75	(10-49)
B* NEW 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	5.95	(10-49)
		TT1.5-1	1.5	.075-500	.075-500	.2-100	.1-50	4.95	(10-49)
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	5.25	(10-49)
		TT4-1	4	.05-200	.05-200	.02-50	1-30	4.95	(10-49)
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	7.95	(10-49)
	TTMO	TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	10.95	(10-49)
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	2.95	(10-49)
		T1-6 NEW	1	.01-150	.01-150	.02-100	.05-50	4.95	(10-49)
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	3.95	(10-49)
		T1.5-6 NEW	1.5	.02-100	.02-100	.05-50	0.1-25	4.95	(10-49)
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	3.95	(10-49)
		T4-6	4	.02-200	.02-200	.05-150	.1-100	3.95	(10-49)
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.45	(10-49)
		T16-1	16	.3-120	.3-120	.7-80	.5-20	3.95	(10-49)
		T36-1	36	.03-20	.03-20	.05-10	.1-5	5.95	(10-49)
	TH	T1-1H	1	8-300	8-300	10-200	25-100	4.95	(10-49)
		T9-1H	9	2-90	2-90	3-75	6-50	5.45	(10-49)
		T16-1H	16	7-85	7-85	10-65	15-40	5.95	(10-49)
	TMO	TMO1-1	1	.15-400	.15-400	.35-200	2-50	4.95	(10-49)
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	6.75	(10-49)
		† TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05.20	6.45	(10-49)
		† TMO4-6	4	.02-200	.02-200	.05-150	.1-100	6.45	(10-49)
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	6.45	(10-49)
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	6.45	(10-49)
		TMO1.6-1	16	.3-120	.3-120	.7-80	5-20	6.45	(10-49)
D 	T	T2-1	2	.025-600	.025-600	.05-400	.5-200	3.45	(10-49)
		T3-1	3	.5-800	.5-800	.2-400	—	4.25	(10-49)
		T4-2	4	.2-600	.2-600	.5-500	.2-250	3.45	(10-49)
		T8-1	8	.15-250	.15-250	25-200	2-100	3.45	(10-49)
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.25	(10-49)
	TMO	TMO2-1	2	.025-600	.025-600	.05-400	.5-200	5.95	(10-49)
		TMO3-1	3	.5-800	.5-800	2-400	—	6.95	(10-49)
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	5.95	(10-49)
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	5.95	(10-49)
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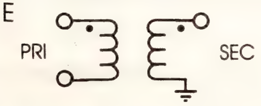
E 	FT	FT1.5-1	1.5	.1-400	.1-400	.5-200	1-100	29.95	(1-4)
	FTB	FTB1-1	1	.2-500	.2-500	.5-300	10-100	29.95	(1-4)
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	29.95	(1-4)
		■ FTB1-1-75	1	.5-500	.5-500	5-300	10-100	29.95	(1-4)

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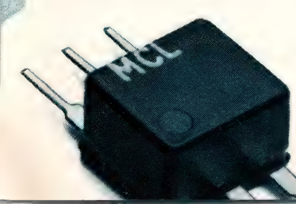
0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

* Maximum Phase Unbalance
1.0° over 1 dB frequency range
5.0° over entire frequency range



CIRCLE NO 162

C72-2 Rev. A

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FAMILY	TYPE	PART NO.	DESCRIPTION/ACCESS TIME	AVAIL.
CMOS Dual Port Static RAM Choices	2K x 8	V61C32	Arbitrated, Busy Flag 55/70/90ns	NOW
	2K x 8	V61C35	Multiplexed 55/70/90ns	NOW
	2K x 8	V61C34	Arbitrated, Semaphore 55/70/90ns	1Q87
	2K x 9	V61C37	Arbitrated, Turbomode 30/35/45ns	4Q86
	1K x 8	V61C30	Arbitrated, Interrupt 55/70/90ns	4Q86
CMOS Dual Port Static FIFO Choices	512 x 9	V61C01	Zero Fall-Through Time 25/35/50ns	4Q86
	1K x 9	V61C02	Zero Fall-Through Time 25/35/50ns	4Q86
	1K x 9	V61C03	Zero Fall-Through Time 15/20/25ns	4Q86

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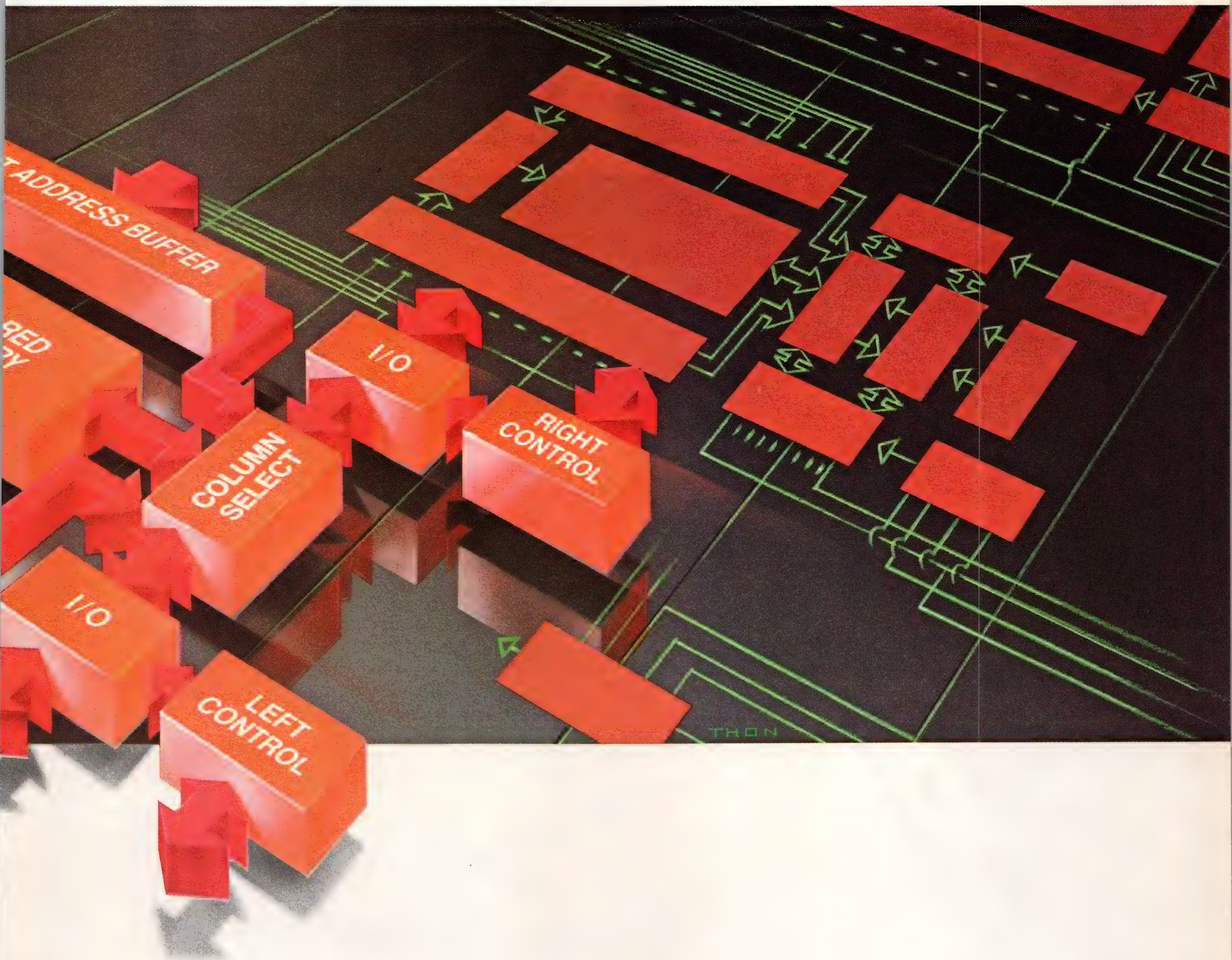

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CIRCLE NO 191

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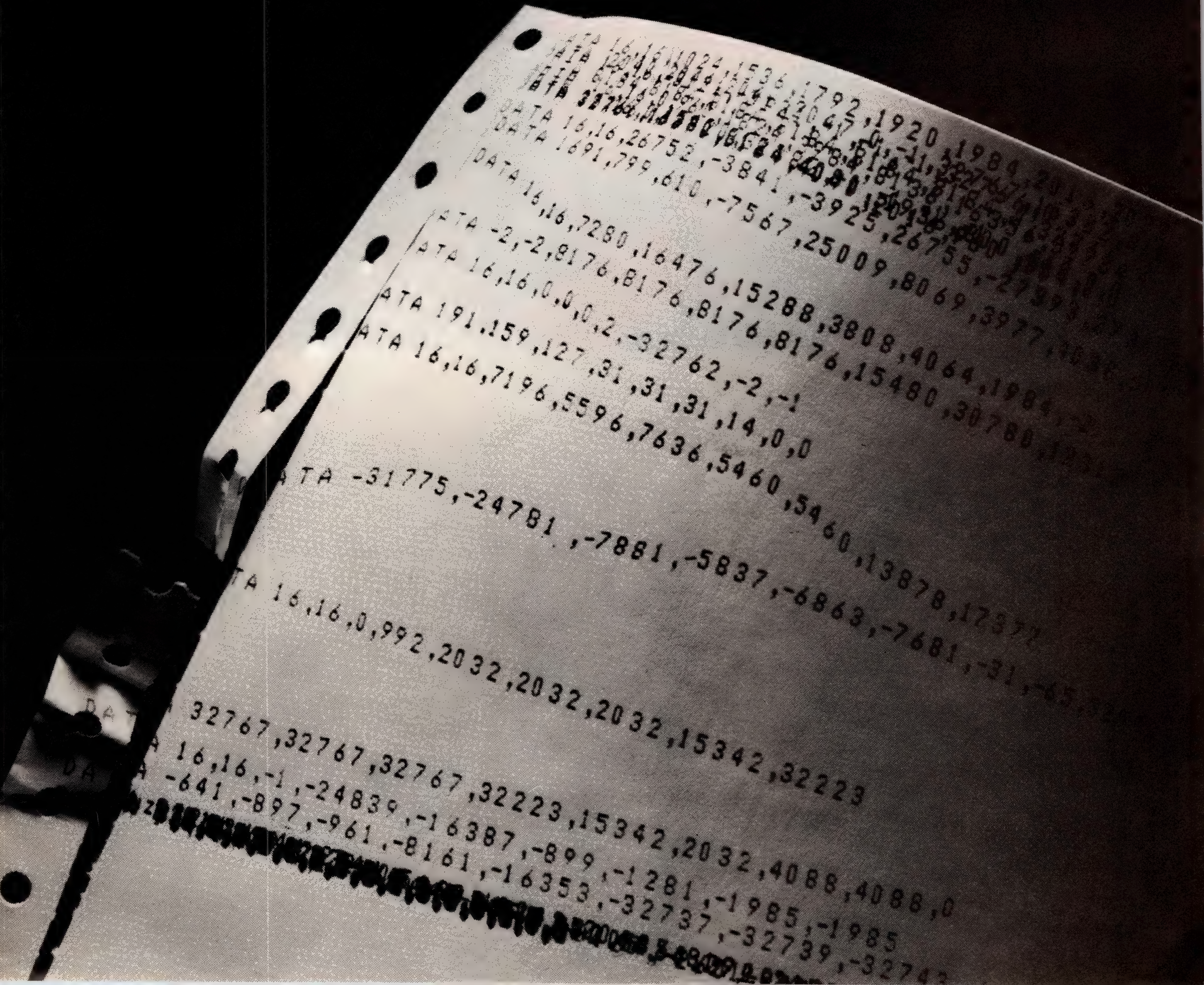

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DATA 16,16,26752,-3841,-3925,26755,-273
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ATA 16,16,0,0,0,2,-32762,-2,-1
ATA 191,159,127,31,31,31,14,0,0
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TA 16,16,0,992,2032,2032,2032,15342,32223
DATA 32767,32767,32767,32223,15342,2032,4088,4088,0
A 16,16,-1,-24839,-16387,-899,-1281,-1985,-1985
DA A -641,-897,-961,-8161,-16353,-32737,-32739
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omp, chomp, chomp.

It's going beautifully.

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Tractor failure.

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We've been the world's premier custom formulator of reinforced, lubricated and other modified engineering plastics virtually since the first ones were created.

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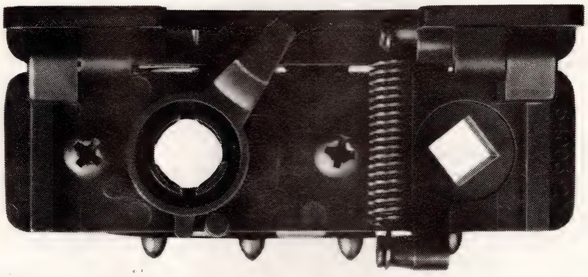

This paper tractor by Precision Handling Devices offers superior dimensional stability and excellent wear resistance to paper dust abrasion. The reason? Virtually every part is created from an easy-to-mold LNP polycarbonate composite.

And there are as many success stories such as this as there are needs for LNP's legendary expertise. Whether you're looking for plastic that's easy to mold, or has low warp, or high strength-to-weight ratios, or is anti-static, or dissipates it. Or, yes, all of the above. The fact is, if we haven't already solved your problem for someone else, we'll be the first to solve it for you.

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LNP

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CIRCLE NO 160

SIGNALS & NOISE

Social issues are of concern to engineers

Dear Editor:

I am writing to express my pleasure at seeing the stimulating article "As engineers' social consciousness matures, concerned groups act as the guiding light" (EDN, July 10, pg 293). The article raises many important issues that are of concern to many technical people such as myself.

As a technical consultant, educator, and member of the IEEE and the ACM, I have long felt that it is important to integrate our profession with broader social issues. Engineers should note that lawyers and accountants are often expected to donate "pro bono" services to community groups on a regular basis. Perhaps it is time for us high-tech professionals to consider giving something back to society in a similar manner.

Thank you again for a timely and important article. I hope to see these issues explored further in EDN.

Sincerely yours,
David Bellin
Flushing, NY

"I FINALLY WORKED OUT ALL THE BUGS. UNFORTUNATELY, IT TURNED OUT THEY WERE TERMITES."

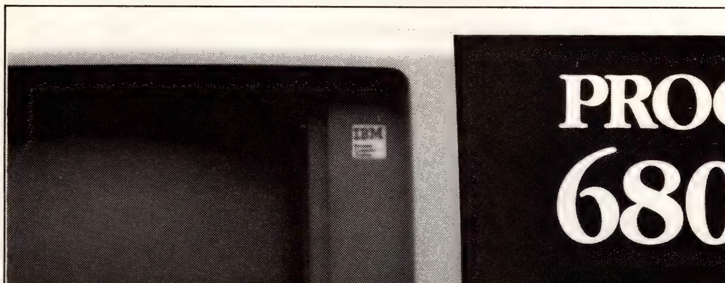
Management must support defensive programming

Dear Editor:

I have just finished reading the article "Defensive programming simplifies program maintenance" (EDN, August 7, pg 157). The article was very informative, but I feel it is incomplete in not mentioning the need for management to make a commitment to adopting defensive programming techniques.

It's very easy for a programmer or team of programmers to abide by the suggested guidelines in the early stages of a long project. However, as the completion date nears, new features must be added, bugs must be fixed, etc; it becomes too easy to forgo the discipline and get the project out the door as soon as possible, usually to satisfy management.

I believe a commitment on the part of managers to enforce the im-



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*Field experience measured on 200 Ridge 32 systems

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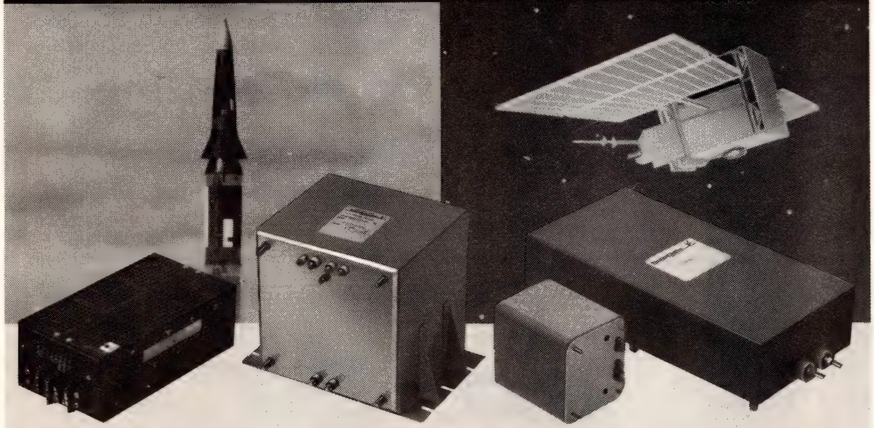

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CIRCLE NO 10

plementation of this kind of programming at all phases of a project is essential to reaping the benefits. If a program is well commented, but the comments no longer describe the code, the effort has been wasted.

Sincerely yours,
Charles P Schultz
Anilam Electronics
Miami, FL

Corrections

Tektronix Inc was inadvertently omitted from the manufacturers list accompanying the article "High-voltage circuits use mixed processes, fulfill diverse roles" (EDN, July 10, pg 74). You can contact the company at the following address or circle the appropriate number on the Information Retrieval Service card.

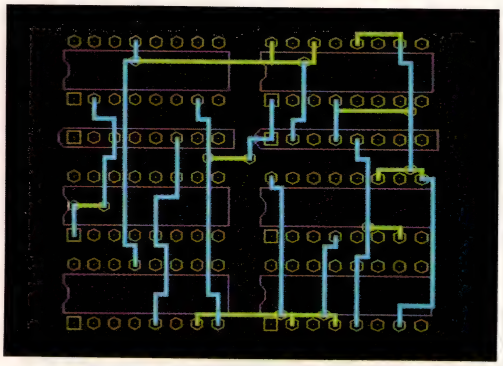
Tektronix Inc
Box 500
Beaverton, OR 97077
(503) 627-2515
Circle No 700

Also please note that the photo accompanying the article "LVDT interface chip's functional blocks offer versatility" (EDN, May 29, pg 159) is not that of the author, Zahid Rahim of Signetics Corp, but that of another Signetics employee. The wrong photo was supplied with the article.

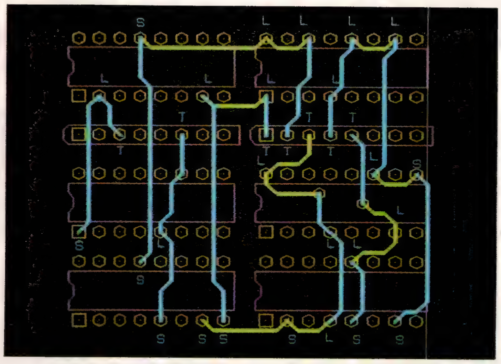
YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

THIS ECL DESIGN PROBABLY WON'T WORK THE WAY THE ENGINEER PLANNED.



THIS ONE WILL.



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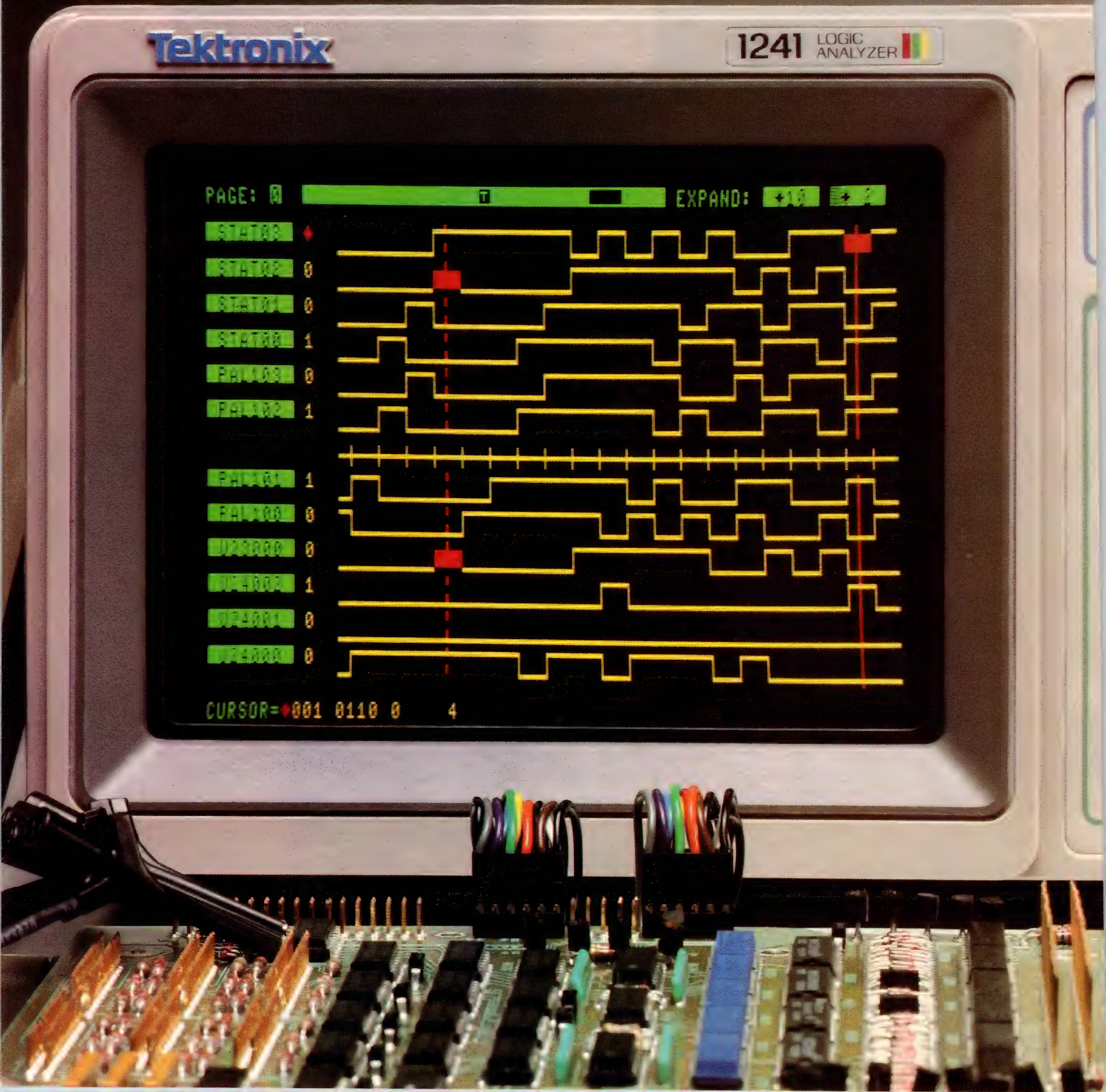
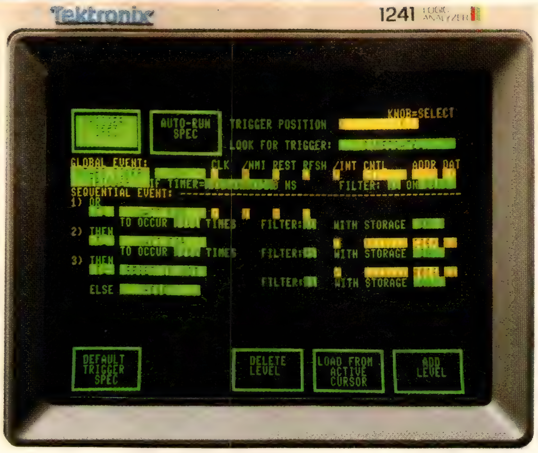
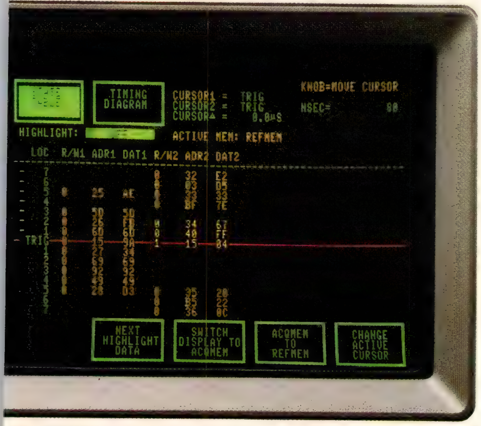




Meet the new 1241—one more reason why Tek's versatile 1200 Series offers you the best of the leading logic analyzers:

1 The 1241's color interface quickly guides your eye to the most relevant information. Analysis is faster. Easier on the eyes. You are more accurate, more productive. For extra readability, a vertical expansion feature doubles the height of the timing diagrams.

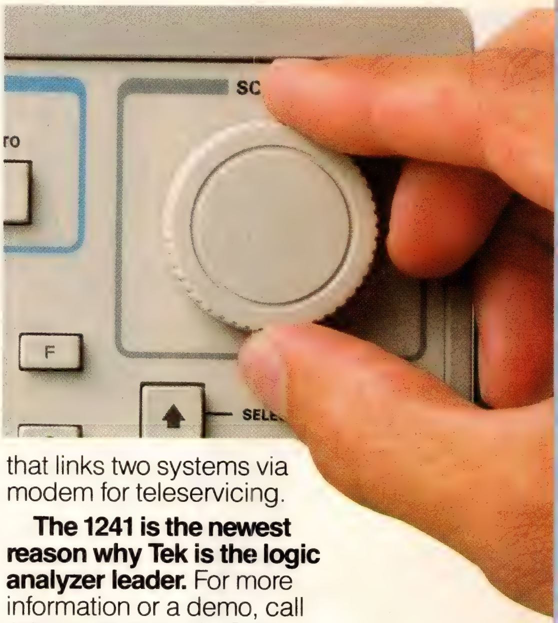
2 Like all members of the 1200 Series, the 1241 clearly shows what your hardware and software are doing at the same time. For integrating partitioned designs, only the 1200 Series' Dual Timebase feature accurately depicts real-time interactions between independently-clocked modules. This lets you monitor relationships between two processors, or between hardware and software. Combine Dual Timebase with performance analysis on the 1241 to analyze the entire system and software performance. Monitor, for example, the range of time spent by one processor waiting for a service request response from a second processor. The 1241's histogram display and 10ns resolution make these measurements clear and precise.



3 For both hardware and software analysis, Tek offers unsurpassed triggering. Software problems are pinpointed by 14 levels of conditional triggering combined with data and program flow qualification. Triggering on the timing characteristics, as well as the state of the hardware activity, is made possible by counters, timers, and duration filters.

4 Ease of use extends beyond the color screen. Four distinct levels of operation add features as your design challenges require. A unique touch-screen menu display lets you select over 50 high-level commands right off the screen. The big front panel knob provides flicker-free scrolling.

5 Modular, expandable and versatile, Tek's 1200 Series keeps costs low and compromises few. Support for all major microprocessors includes three types of disassembly. With 14 combinations of 9- or 18-channel acquisition cards, you configure the best data width (up to 72 channels), memory depth (up to 2K) and sample rate (up to 100 MHz). Add ROM packs for data analysis; RAM packs for storage; COMM packs for RS-232 and GPIB links to computers, plus printer interfacing; and master/slave capability that links two systems via modem for teleservicing.



The 1241 is the newest reason why Tek is the logic analyzer leader. For more information or a demo, call 1-800-245-2036. In Oregon, call 231-1220. Or contact your local Tek Sales Engineer.

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CALENDAR

Computer Security and Access Control, Milwaukee, WI. Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N Sixth St, Milwaukee, WI 53203. (414) 224-3952. November 5 to 6.

Optical Storage for Small Systems, Los Angeles, CA. Technology Opportunity Conference, Box 14817, San Francisco, CA 94114. (415) 681-3700. November 5 to 7.

ICALEO '86 (International Congress on Applications of Lasers and Electro-Optics), Arlington, VA. ICALEO '86, 5151 Monroe St, Suite 102W, Toledo, OH 43623. (419) 882-8706. November 10 to 13.

IEEE ICCAD '86 (International Conference on Computer-Aided Design), Santa Clara, CA. MP Associates, 7366 Old Mill Trail, Suite 101, Boulder, CO 80301. (303) 530-4562. November 10 to 13.

Comdex/Fall, Las Vegas, NV. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. November 10 to 14.

Digital Signal Processing, Single-Chip DSP and Parallel Processors—Theory, Design and Applications (short course), Anaheim, CA. DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. November 10 to 14.

Defense Data Network and Department of Defense Protocol Standards (short course), College Park, MD. University of Maryland, College Park, MD 20742. (301) 985-7122. November 11 to 13.

Government Microcircuit Applications Conference, San Diego, CA. Palisades Institute for Research Services, 201 Varick St, Suite 1140, New York, NY 10014. (212) 620-3371. November 11 to 13.

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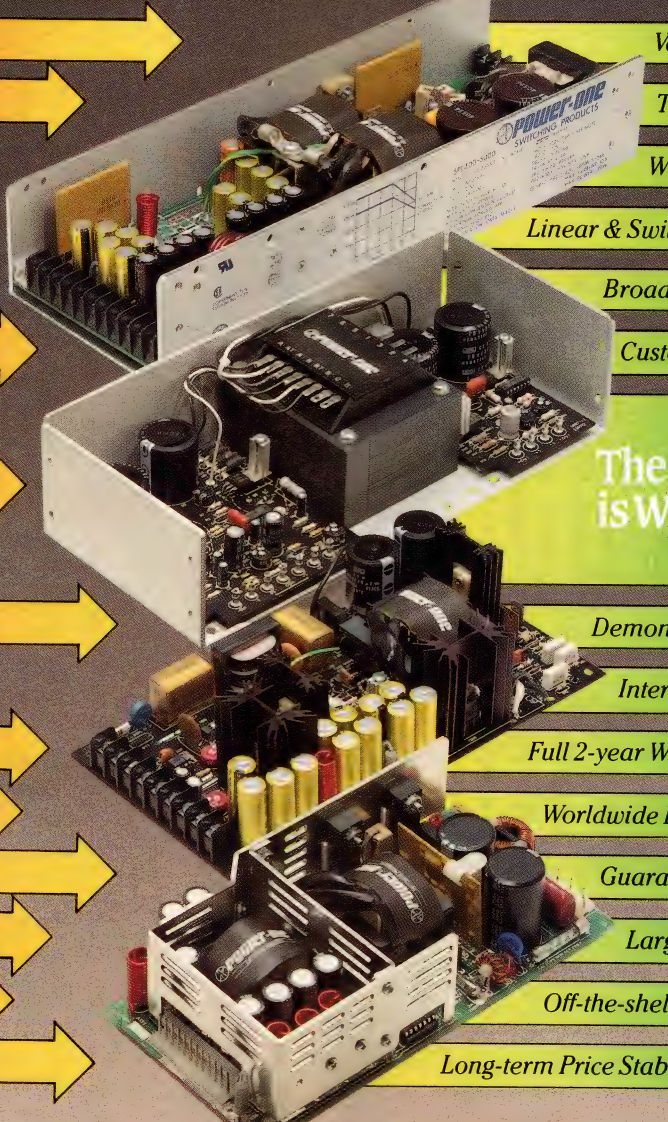

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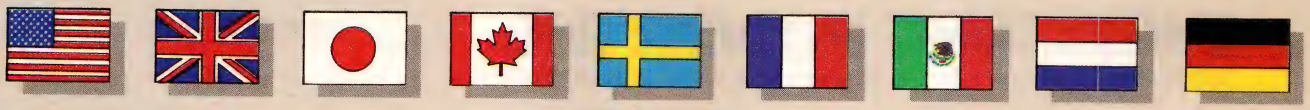

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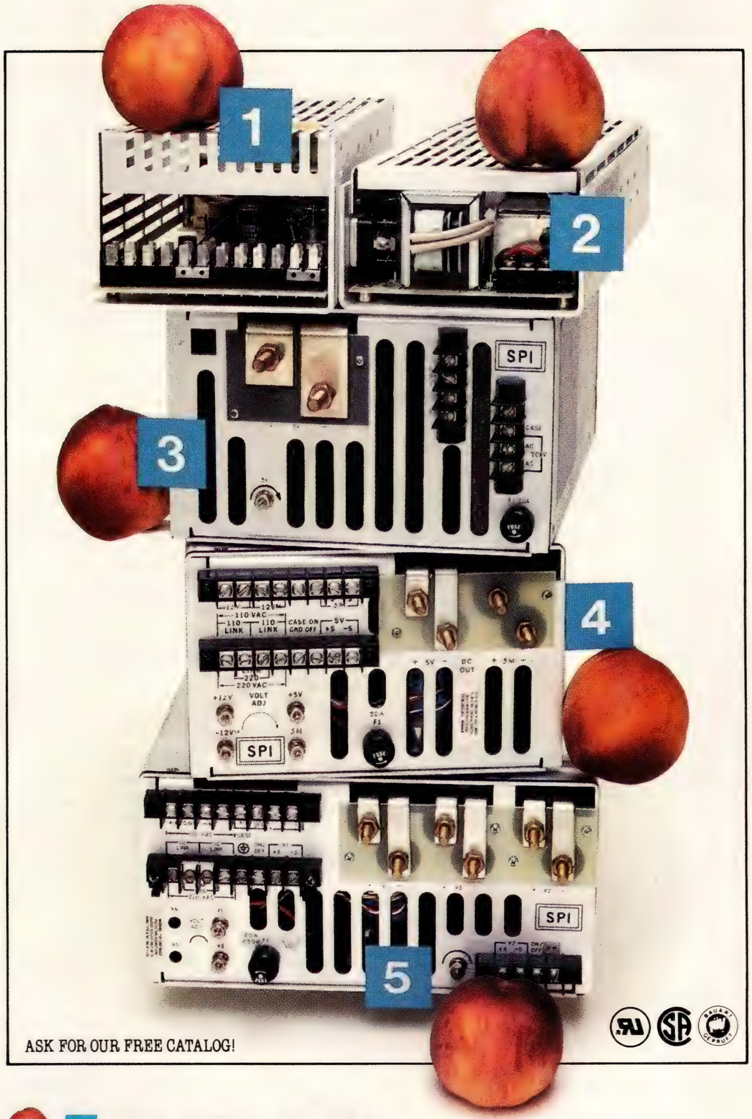

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Autofact '86, Detroit, MI. Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. (313) 271-1500. November 11 to 14.

Design and Drafting of Printed Circuits (short course), Milwaukee, WI. Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N 6th St, Milwaukee, WI 53203. (414) 224-3952. November 11 to 14.

Real-Time Operating Systems: A Hands-On Workshop, Palo Alto, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. November 11 to 14.

Electronica '86, Munich, West Germany. Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07540. (201) 652-7070. November 11 to 15.

Northeast Lightwave Expo, Boston, MA. Lightwave, 235 Bear Hill Rd, Waltham, MA 02154. (617) 890-2700. November 12 to 14.

Analog Applications Seminar, Long Island, NY. Precision Monolithics, 1500 Space Park Dr, Santa Clara, CA 95054. (800) 843-1515; in CA, (800) 826-9664. November 13.

Federal High Technology, San Francisco, CA. Foresight Science and Technology, 2000 P St NW, Suite 305, Washington, DC 20036. (202) 833-8844. November 13 to 14.

India International Trade Fair, New Delhi, India. Mr Jha, Counselor of Commerce, Embassy of India, 2107 Massachusetts Ave NW, Washington, DC 20008. (202) 939-9841. November 14 to 30.

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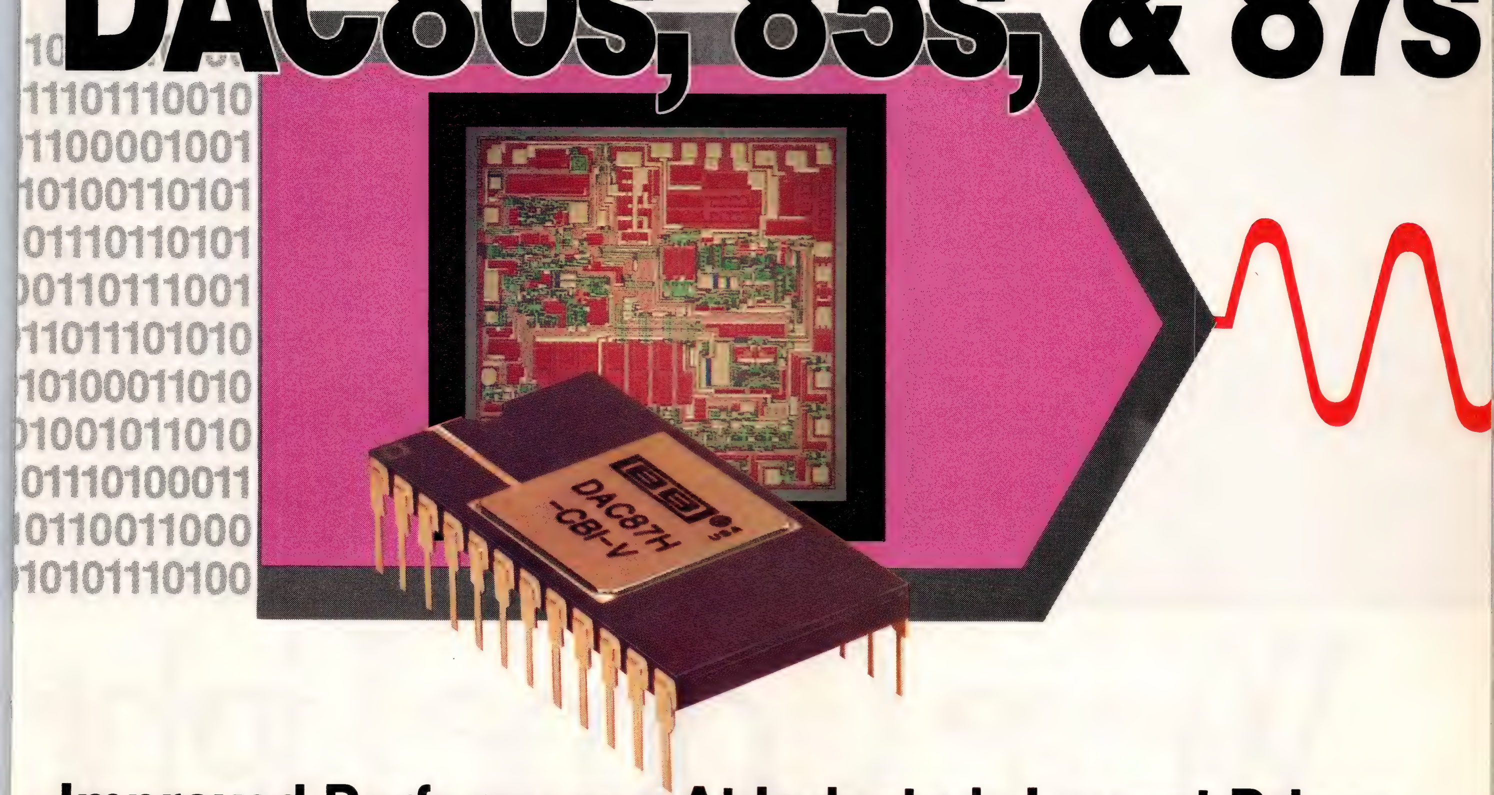

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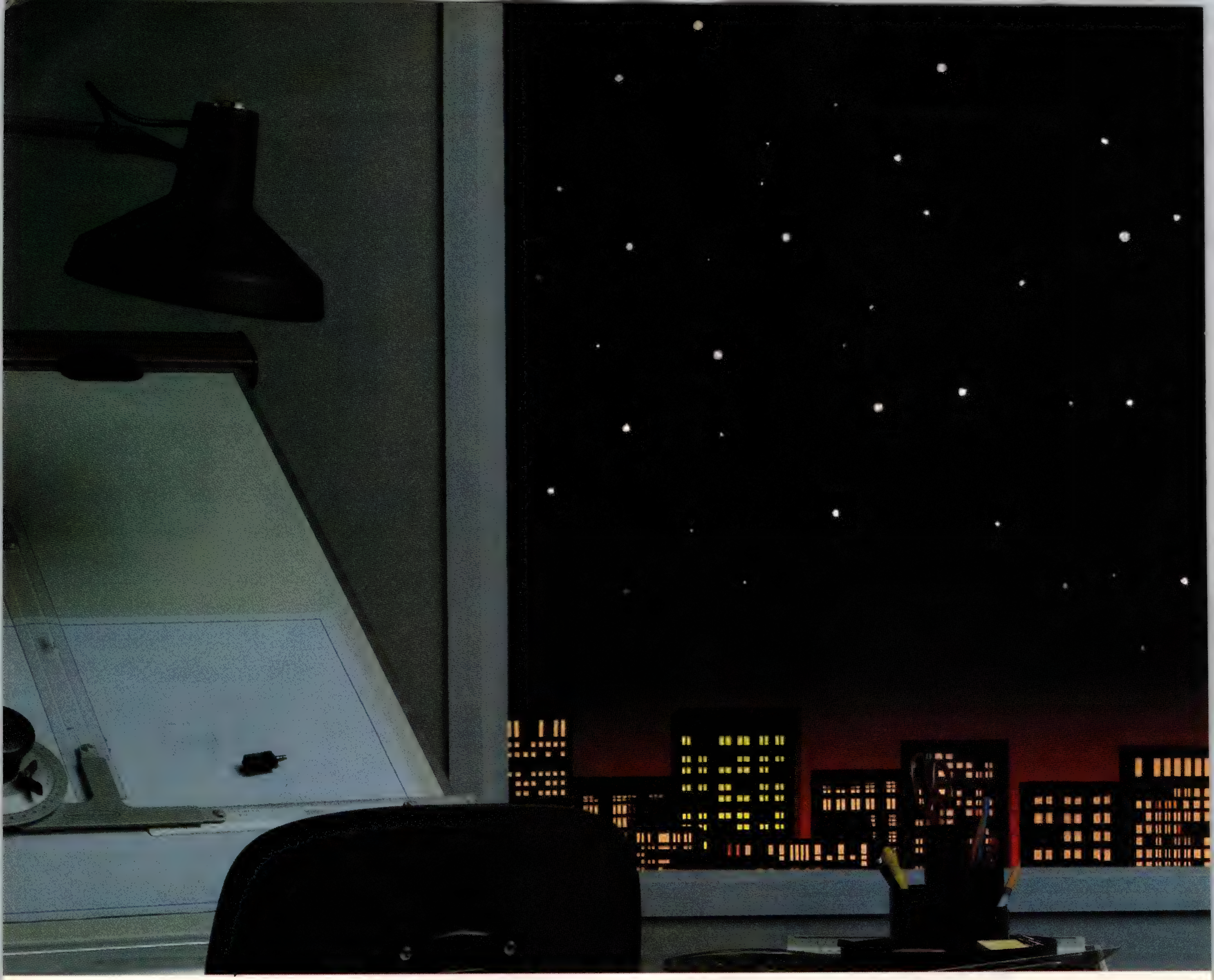

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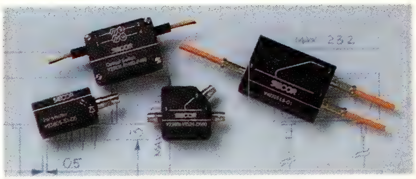

Left to right: 200 MBaud transmitter, fiber optic switch, WDM, T-coupler with pigtail.

SIECOR

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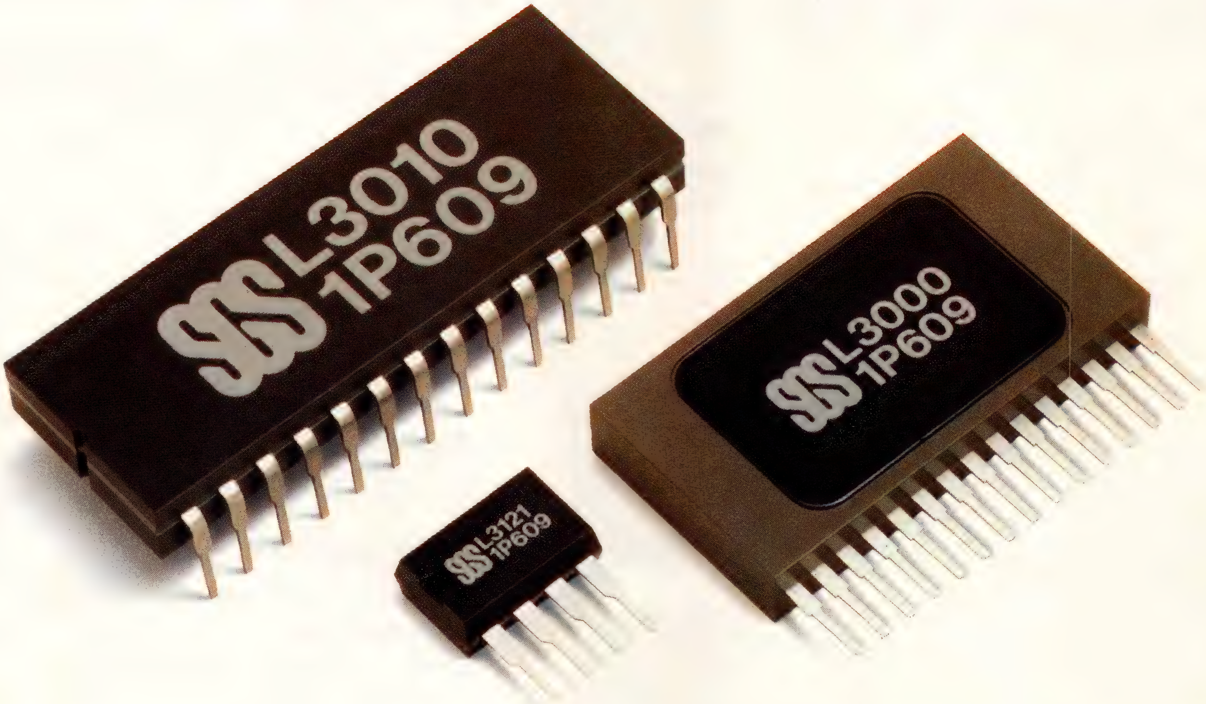
We Did It

The Integrated SLIC From SGS



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EDITORIAL

Hold the pickle

"If we are to . . . put our citizens back to important *work (not working at Burger King), it is necessary to recognize the closed circle on which our living standard is based. Engineering leads to manufactured products. Manufactured products, in turn, lead to research and development. Research and development leads to more engineering."—Irwin Feerst, Committee of Concerned EEs*

My friends Mary and Joe, engineering and marketing managers, respectively, for a large American electronics company, took me to lunch yesterday. I was surprised when we went by subway to Burger King.

"What gives?" I asked. "Trade-press editors used to be wined and dined at the Ritz."

"Business is terrible," Joe said. "We just don't have the big entertainment budgets anymore. The only bright side is that our competitors can't take you to the Ritz either."

I contemplated the menu and didn't see any bright side at all. "Well, I understand that the manufacturing has all gone overseas," I said, "but surely you're making tremendous profits selling your engineering services and licensing the technologies you develop."

"Well, that game worked for a while," Mary said. "But now, Korean engineers perform exactly the same quality of services that my staff did but at 50 to 55% of the going hourly rate. So we've cut way back. See that assistant manager behind the counter? He used to be my best engineer. Could you order? I can't face him."

I approached the assistant manager. "Three burgers."

"Standard burgers?"

"Well, hold the onion on mine."

He pulled a drawing of a standard burger from a stack of drawings and used a red pen to cross out the onion. "If you'll initial this, I'll get it right off to drafting. How about the other two burgers?"

"I'll check with my guests." I realized I would pay for lunch because Joe had paid the subway fare.

"Well," the assistant manager said, "if you think there's a good chance they'll go for standard models, you might want to put the order through. I'm afraid we're quoting delivery at 20 to 25 minutes ARO, but we can make minor changes without delay. Besides, you don't want your burger coming out before theirs."

"Don't you have a just-in-time program that would allow our burgers to be finished at the same time?"

"Sorry, the people who understand those types of things still have jobs in electronics."

"I understand. OK, put the order through," I said. The lunch hour was going fast. Meanwhile, the final drawings on my own burger came back from drafting; he handed them off to manufacturing.

I returned to the counter several minutes later after consulting Mary and Joe. I told the assistant manager, "On one of those two burgers, we just want extra ketchup. On the other, hold the tomato, add extra onion, and make it medium rare. Any problem?"

"Well, they're already in manufacturing," he said. "The first one should be no problem, though. I suggest a field retrofit. You can just get one of these little packets of ketchup and install it yourself. It's not UL listed for field installation, but it's designed to meet all the applicable UL specs."

"OK, we'll risk it. An engineering manager will be handling the installation. But how about the other one?"

"That could be a problem," he said, entering a few keystrokes on a computer terminal. "The tomato and onion we can handle with an engineering change order, but it's too late for the medium rare. Our R&D staff is working on a technology that would reverse the cooking process, but commercial applications are several years off. Would medium be OK?"

"Well, the order came from a marketing manager, and marketing usually has the final say. Better scrap the existing medium burger and start over," I said.

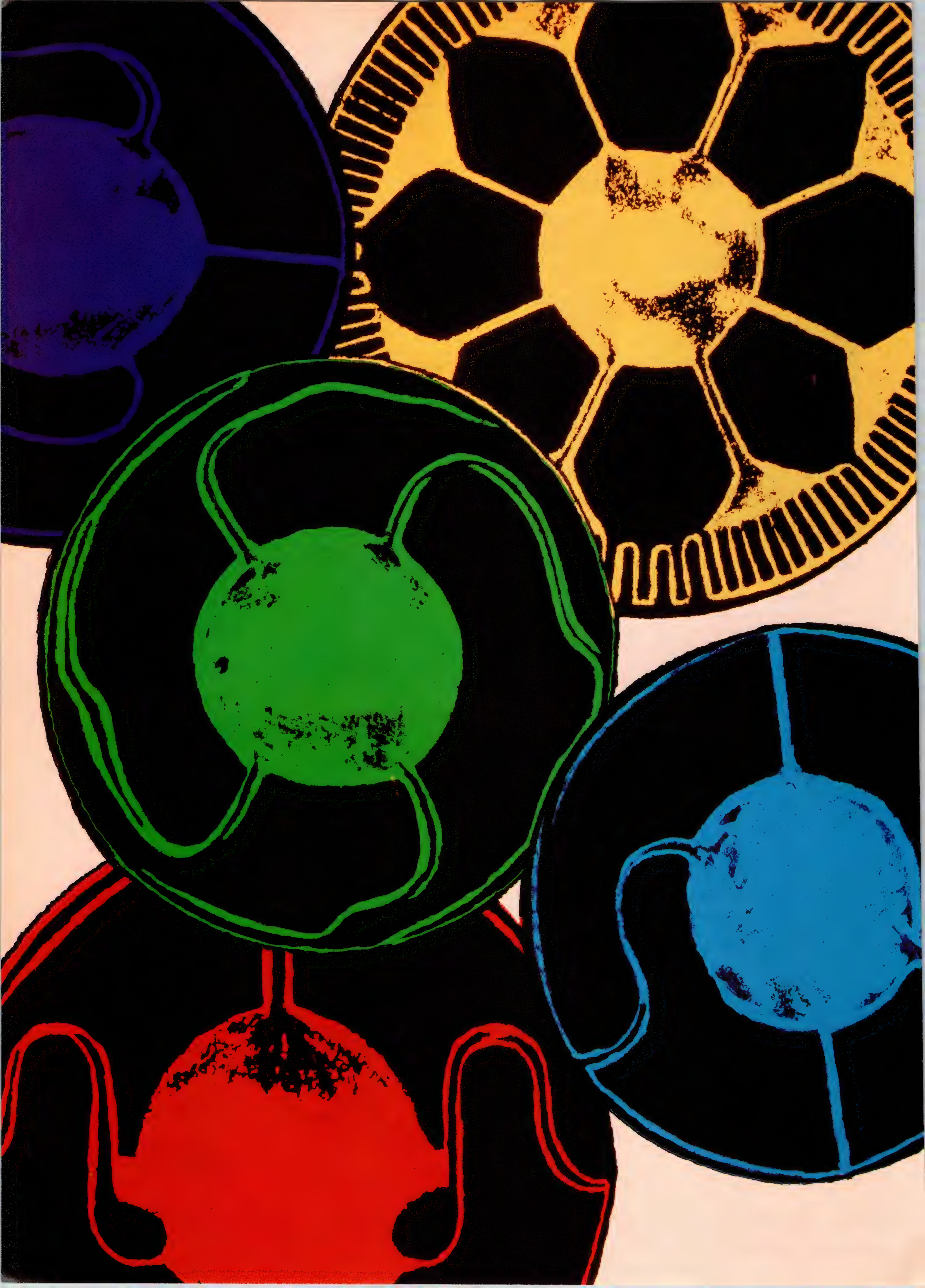
Later, Joe enjoyed his warm burger, while Mary and I choked down our cold ones.

"With business so bad, what are the prospects for you two?" I couldn't help asking.

"Grim," they said. "We've both applied for jobs here. We hope that more assistant-manager slots open up soon."

Rick Nelson

Rick Nelson
Managing Editor



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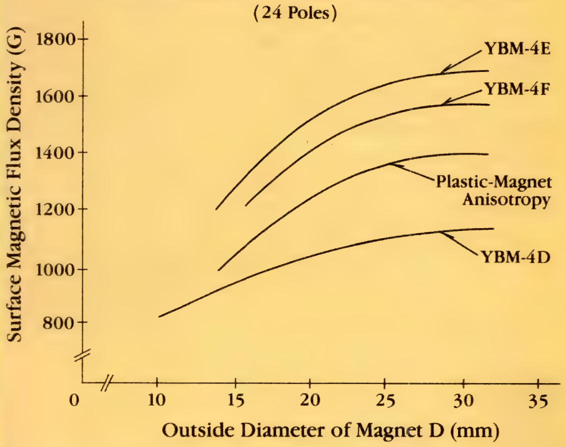

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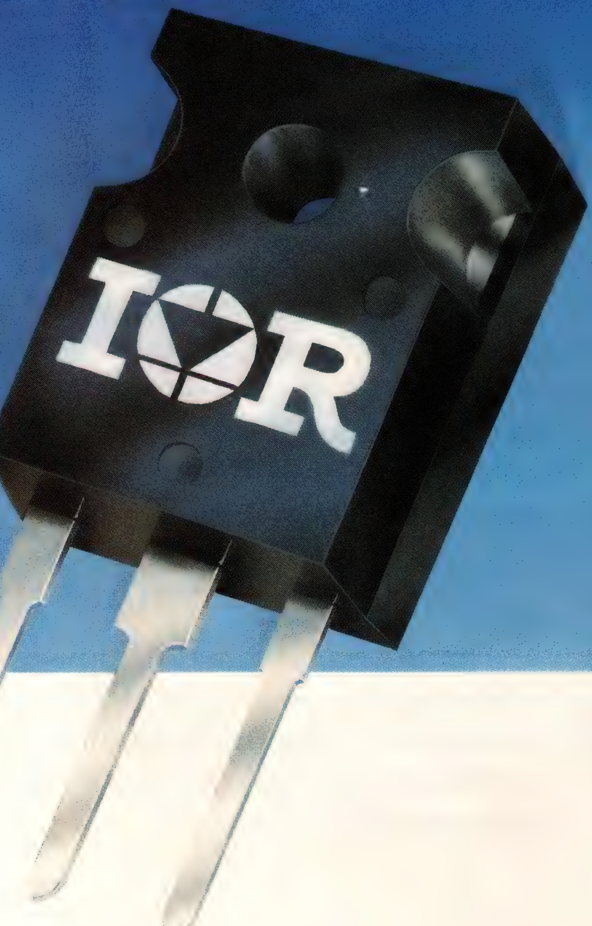

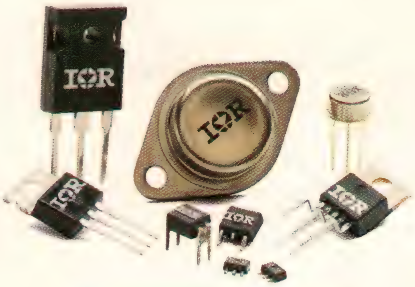

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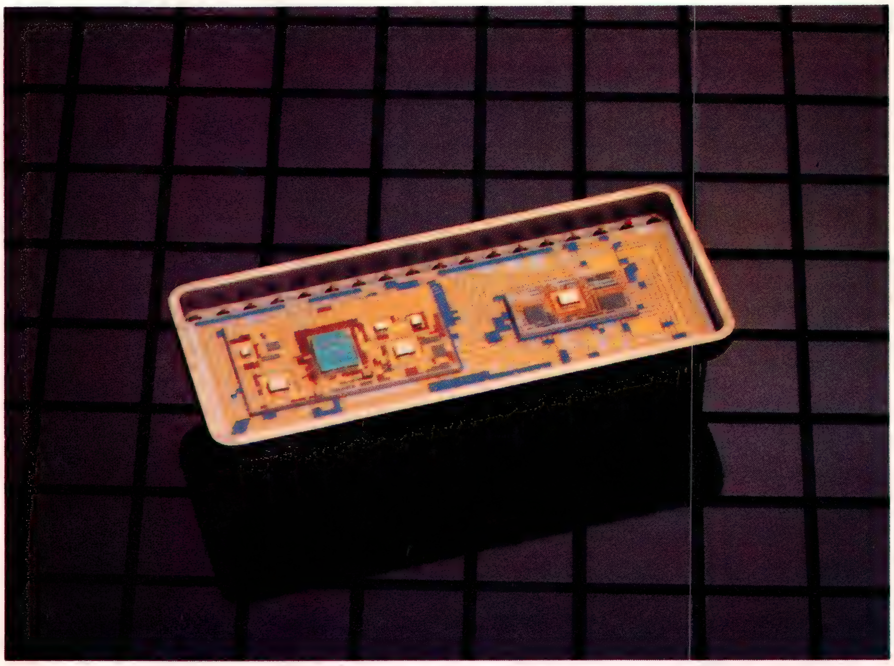
Synchro/resolver converters bring low cost and small size to motion-control systems

Tarlton Fleming,
Associate Editor

Modular and hybrid converter microcircuits are making the synchro/resolver (S/R) approach to angle measurement increasingly attractive. S/R-to-digital and digital-to-S/R converters—in particular the hybrid type—are smaller and less expensive than they used to be, thanks to the inclusion of custom CMOS ICs, yet their performance suits a broad range of military and industrial applications. Noteworthy features of these hybrids are 5V operation, programmable resolution to 16 bits, and tachometer-grade velocity-voltage outputs that let you eliminate expensive electromechanical tachometers. Modular converters retain the advantage of higher accuracy, especially at high resolution (18 bits and up).



Hybrid converters are creating new markets *for motion-control systems based on synchros and resolvers. This 16-bit digital-to-synchro (or -resolver) converter, Model HDSR2056 from Natel Engineering, provides analog signals representing a shaft's angular position within ±1 arc-minute.*

All-analog synchro systems have been used aboard ships since World War II (see **box**, "What are synchros and resolvers?"). Before and after the proliferation of digital computers, synchros have helped to monitor and control the propellers' rpm, the rudder's position, and the radar and gun turrets' positions, among other things. To control these loops by computer, though, the system must include synchro converters to translate data between the analog and digital domains. (In this article, the term S/R converters includes both the S/R-to-digital and the digital-to-S/R types. Some products are dedicated to synchro-format signals, some are dedicated to the resolver format, and others can accommodate either format.)

Military consumption of S/R converters has traditionally been vastly greater than industrial consumption, but industrial use is likely to grow, according to Analog Devices' marketing engineer Ian Bruce. He sees in particular a prospect for increasing use of resolver-to-digital converters, both to retrofit existing systems based on optical-encoder transducers, and to serve a new market—the use of resolvers in controlling brushless ac and dc motors.

Brushless motors currently use Hall-effect transducers with 1% accuracy to help commutate the field windings. A resolver and a 12-bit resolver-to-digital converter, however, can do this job with 0.024% accuracy. Analog Devices' 12-bit 1S24 resolver-to-digital converter, for instance, can track a shaft at 170 revolutions/second, and the company's 10-bit 1S14 can track at 680 revolutions/second. In addition, these converters provide absolute shaft-position information for precise computer control, and a velocity-voltage output to stabilize the control loop.

High-grade velocity-voltage outputs represent a major advance in the design of S/R converters. Most tracking converters—the most common type of S/R converter—employ a type-II servo loop (two integrators in the feedback path), which generates the velocity voltage as a by-product of its operation. In the older converters, this output is uncontrolled and may have an error tolerance of ±10% or higher. But recent products from Analog Devices (the 1S14 Series and the 1S74) and ILC Data Device Corp (the RDC-19200) achieve velocity outputs having 1% or better accuracy.

Because these velocity outputs are comparable to those from tachogenerators, you can simply omit the tachogenerator from your system. In its place, the converter supplies a voltage that is a linear function of angular velocity, scaled to ±10V at maximum rpm (using ±15V supplies), and is well behaved near 0V, where the circuit must distinguish between clockwise and counterclockwise rotation. Moreover, both firms thoroughly characterize this output, which marks a departure from past practice. Output specs include linearity (±0.1% typ), zero offset (±0.25 mV typ for the ILC parts, ±0.5 mV typ for the Analog Devices parts), and temperature coefficients of scale factor (200 ppm/°C max) and zero offset (50 μV/°C max).

Besides accurate velocity outputs, the 1S74 and RDC-19200 resolver-to-digital converters provide digitally programmable resolutions

What are synchros and resolvers?

Synchros and resolvers are electromechanical components that resemble small ac motors in appearance. They find wide application as shaft-angle transducers, both to sense and to control the angular position of rotating shafts. They come in standard cylindrical housings ranging from size 5 (0.5 in. in diameter) through sizes 8, 10, 11, 15, and 23 (2.3 in. in diameter).

To monitor a shaft angle with either type of device, you apply an ac reference waveform to the rotor winding. Transformer action then produces in-phase ac voltages across the stator windings, whose rms amplitudes represent the shaft angle. (Older resolvers used wear-prone slip rings and brushes to connect a reference signal to the rotor. Because modern brushless resolvers include a small built-in transformer that inductively couples a reference signal to the rotor, these units' life expectancy depends mainly on the quality of their ball bearings.)

A resolver has two separate stator windings, oriented at 90° to one another, that provide a unique ratio of rms amplitudes for each shaft position within a full revolution. A synchro has three stator windings connected in a Y configuration, physically oriented at 120° intervals. Together, the three rms-amplitude outputs (taken across the three output terminals, two at a time) provide a unique combination for every shaft position within 360° of rotation.

Selsyn to synchro

These devices—also referred to as rotary-angle transducers—are descendants of the selsyn (self synchronous) motor generators developed in the 1920s. The US Navy began using selsyns in large quantities during World War II, renaming them synchros to avoid a manufacturer's trade name. Many of these units were large and able to deliver considerable torque to a load. Later, though, the use of servo control loops provided power amplifiers and motors to drive the load, and that control method has relegated the synchro to its present role as primarily a signal generator and receiver.

Today, synchros remain in demand largely because of entrenched use by the Navy. Where this commitment to existing systems and inventories doesn't exist, however, the more versatile resolver can offer an advantage. Because the resolver's two output amplitudes correspond to the sine and cosine of its shaft angle, they can connect directly to the input of a converter. (All S/R converters operate internally on resolver-format rather than synchro-format signals.) Also, the resolver's outputs are directly usable in analog-computing operations such as the transformation of polar to rectangular coordinates.

Basic variants of the synchro

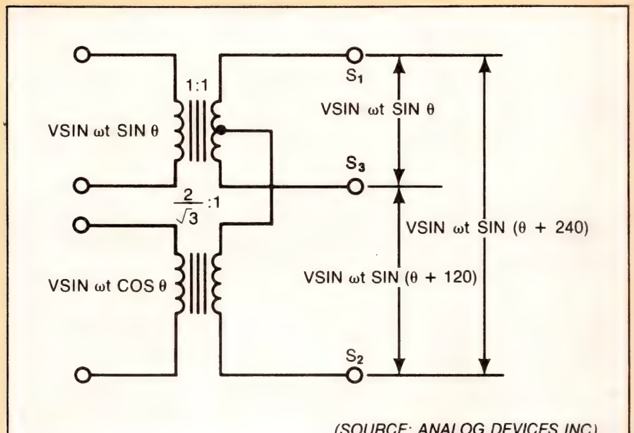
You can easily convert the 3-wire output of a synchro to a 4-wire resolver output (and conversely) using a Scott-T transformer **(Fig A)**. You'll find these transformers at the input of all synchro-to-digital converters, for example. Indeed, Scott-T transformers allow synchros to do everything a resolver does, while adding only a few seconds of angular error to the operation.

Variations of the basic synchro idea solve a variety of motion-control problems. These variants include the synchro control transmitter (CX), which generates angle information on its stator windings as you turn the shaft, and the synchro control transformer (CT), which is used as a nulling device in servo loops.

The CT generates on its rotor winding a signal that's proportional to the sine of the difference between its shaft angle and an angle represented by synchro signals applied to its stator windings. Yet another synchro variant, the control differential transformer (CDX), is similar in function to the CT, except that its rotor output is a 3-phase synchro signal. You can choose resolver components analogous to each of these synchro types.

Besides the angle-transducer synchros just described, you can choose from a selection of so-called torque synchros, whose rotors can drive an of 10, 12, 14, or 16 bits. This feature lets a system combine 16-bit-fine positioning accuracy with fast, 10-bit slewing speed. In addition, Analog Devices has pioneered the use of small transformers (picotransformers) in its resolver and synchro converters. Wound with 50-gauge wire, these tiny Scott-T and reference-isolation transformers offer 500V galvanic isolation and fit within a standard 32-pin hybrid package.

Another industrial application involves the substitution of resolvers for optical shaft encoders. Optical encoders are capable of greater accuracy than resolvers at a given resolution, and they don't require separate digitizing electronics. Optical encoders are less rugged, however, and they cannot match the resolver's operating-temperature range. For many applications, you



(SOURCE: ANALOG DEVICES INC)

Fig A—The Scott-connected (or Scott-T) transformer *converts resolver signals to the synchro format, and vice versa.*

indicator dial or other light load in response to signals applied to the stator windings. Resolvers are not available as torque components.

Synchros and resolvers also come as 2-speed systems (coarse and fine) that provide greater resolution and accuracy than a single-speed system can deliver. In one form, separate coarse and fine resolver units are geared together so that the fine resolver's shaft rotates, say, 36 times for one revolution of the coarse resolver's shaft. (Shaft-turns ratios of 1:36 and 2:36 are common in aerospace applications; binary ratios of 1:8, 1:16, and 1:32 are used in aerospace and industrial systems.) In a form that avoids gear backlash and mechanical wear, the coarse and fine resolvers have a common shaft; multiple poles (windings) in the fine unit generate the required multiturn output electrically.

The linear or rotary Inductosyn (a registered trademark of Farrand Industries of Valhalla, NY) is another option for high-accuracy motion control. Used in the numerical-control and machine-tool industries, these resolver-like devices can achieve accuracies of ±0.0001 in. (linear) and ±0.5 arc-second (rotary).

A linear Inductosyn consists of a fixed scale and a movable slider, separated by about 0.005 in. You apply a 5- to 10-kHz low-voltage reference signal to a serpentine printed-circuit pattern on the scale. This signal induces ac signals in two similar pc patterns on the slider, and these patterns are physically positioned so that their induced voltages are always in quadrature.

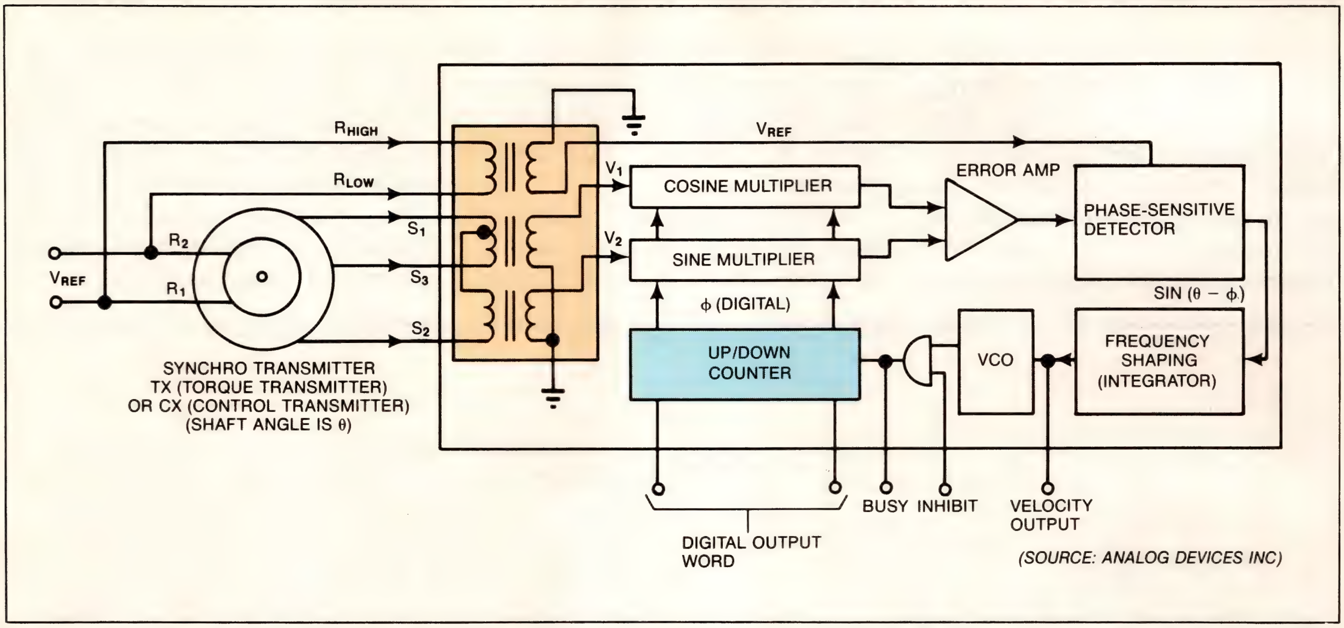
The Inductosyn's output signals thus resemble those of a resolver, but the relatively low magnetic coupling between the scale and the slider results in much lower (20 mV) signal amplitudes. A preamplifier must boost these levels to about 2.5V rms before they can drive a resolver-to-digital converter. When you do incorporate the preamp, the converter's full range (4096 counts at 12 bits, for example) represents slider motion across one pitch, or cycle, of the Inductosyn's scale pattern.

Watch for error at high rpm

All synchros and resolvers are ac transducers, in which angle information modulates a reference (carrier) signal. Standard reference frequencies include 60, 400, and 2500 Hz; a higher frequency allows the system to track higher angular velocities. The desired carrier modulation results from variation in magnetic coupling between rotor and stator coils as the shaft turns.

Undesired modulation represents error, of course. One source of this error is the voltage that appears in quadrature with the signal at high rates of shaft rotation. Called speed voltage, this potential error signal is created, for example, when a moving rotor coil passes through signal flux from the stator coils.

Tracking S/R-to-digital converters include a phase-sensitive detector that rejects this quadrature voltage—provided the reference and signal inputs are in phase. If they are not, you can add an external RC network for phase compensation. Better yet, among the more recent products you can choose a converter that internally synthesizes an in-phase reference.



(SOURCE: ANALOG DEVICES INC)

***Fig 1—This tracking synchro-to-digital converter's input transformers** isolate the reference signal and convert the synchro transmitter's signals to resolver format. The converter incorporates a type-II servo loop, in which the frequency-shaping integrator derives the shaft velocity from an acceleration signal. A second integrator (the up/down counter) derives the shaft position from the velocity signal.*

should evaluate both approaches, because the advent of low-cost ($100) converters is opening the way to replacement of lower-resolution optical encoders by resolver-converter combinations.

In tracking S/R-to-digital converters **(Fig 1)**, the type-II servo loop forces an up/down counter to track the analog-angle information. Digital outputs from this converter represent the input angle to within ±1 LSB, provided the input data does not exceed the converter's maximum tracking rate.

Track without lag error

Because the converter's tracking capability depends on the maximum pulse rate it can sustain between a voltage-controlled oscillator (VCO) and a counter, lower-resolution converters can follow shaft rotation at a higher rpm; they require fewer pulses per revolution from the VCO. Also, the type-II loop tracks without lag error for any data rate below the converter's specified limit.

Of the available tracking S/R-to-digital converters, Natel Engineering's HSRD1006 is the only one that operates from a single 5V supply. This 16-bit, single-channel hybrid converter dissipates 100 mW, can achieve a 1.3-arc-minute accuracy, and includes a reference-synthesizer circuit that compensates for signal-to-reference phase shifts to ±45°. Furthermore, the device is pin programmable for synchro or resolver inputs and for 16- or 14-bit resolution. The 14-bit mode provides a tracking limit of 10 revolutions/second.

For multichannel resolver-to-digital converters, the successive-approximation method of conversion is preferable to the tracking method because it lets you time-share one converter among the channels. Successive-approximation, multichannel converters employ dual sample/hold amplifiers that simultaneously sample the sine and cosine signals of each resolver channel. The converter then sequentially converts each channel. A successive-approximation converter does generate "stale" data (that is, shaft position can change while the system samples and converts data), and the S/H amplifiers are sensitive to noise, but this approach does cost less than a system using one tracking converter per channel. Multichannel converters are available from most of the major suppliers. They come in hybrid, modular, board-level, and rack-mounted configurations.

To achieve angle measurements with resolution and accuracy exceeding 16 bits, you have several options. If the application permits, a high-resolution optical encoder may be suitable. Alternatively, rugged environmental conditions may dictate a resolver system. In that case, a suitable 2-speed converter combined with a 2-speed resolver or a linear or rotary Inductosyn may do the job. Inductosyn-to-digital and resolver-to-digital converters are functionally identical.

Two speeds for accuracy

A 2-speed resolver or synchro system can provide resolutions to 22 bits, ±10-arc-second accuracy, and ±2-arc-second repeatability. In either case, an appropriate 2-speed S/R-to-digital converter will simultaneously convert the coarse and fine outputs to a word representing the equivalent shaft angle.

You can use a single-speed converter for each type of output (coarse and fine) and then digitally scale and combine the converters' digital outputs. Or you can buy a single module that includes all these functions, such as the Series 168K400 from Control Sciences Inc,

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or the Series 1512 from Transmagnetics. Parts in both series spec accuracies of 16 bits and 20 arc-seconds and accommodate a shaft-turn ratio of 36:1 (among other ratios particular to the respective series).

DSRCs (Digital-to-S/R) converters are easier to realize than the reverse, just as D/A conversion is simpler than A/D conversion. A DSRC is built around two nonlinear

TABLE 1—REPRESENTATIVE SYNCHRO/RESOLVER CONVERTERS

MANUFACTURER AND MODEL	RESOLUTION (BITS)	POSITION ACCURACY (ARC-MINUTES MAX)	TRACKING RATE (REV/SEC MIN)	OUTPUT DRIVE (VA MAX)	PRICE	COMMENTS
ANALOG DEVICES						
1S14*	10	±25	680	—	$192	TACHOGENERATOR OUTPUT; 40-PIN HYBRID
1S24*	12	±8.5	170	—	$195	TACHOGENERATOR OUTPUT; 40-PIN HYBRID
1S61*	16	±10	10.5	—	$175	32-PIN HYBRID
1S74*	10, 12, 14, 16	±4	10.5	—	$342	PROGRAMMABLE RESOLUTION; TACHOGENERATOR OUTPUT; 40-PIN HYBRID
2S20*	12	±11	100	—	$88 (100)	32-PIN HYBRID
AUTOTECH						
M1890-R*	8, 10, 12	±0.2 REPEATABILITY	30	—	FROM $2195	PROGRAMMABLE RESOLUTION; INCLUDES RESOLVER AND A 4×6×10.5-IN. CABINET FOR THE CONVERTER AND DISPLAY
COMPUTER CONVERSIONS						
SDC40ST*	14	±4	10	—	$350	2.6×3.1×0.42-IN. MODULE
DSL40†	14	±4	—	1.5	$350	2.6×3.1×0.6-IN. MODULE
CONTROL SCIENCES						
168K400*	16	±0.33	5	—	$695	2-SPEED CONVERTER; 2.6×3.1×0.82-IN. MODULE
192A600†	12	±21	—	25	$445	5.26×5.38-IN. CARD
ILC DATA DEVICE						
RDC-19200*	10, 12, 14, 16	±1.3	12.5	—	$99 (100)	PROGRAMMABLE RESOLUTION; TACHOGENERATOR OUTPUT; 40-PIN HYBRID
DRC-10520†	16	±1	—	2.0	FROM $325	32-PIN HYBRID
DSC-11520†	16	±1	—	0.024	FROM $210	32-PIN HYBRID; PROGRAMMABLE FOR SYNCHRO OR RESOLVER OUTPUT
INTERFACE ENGINEERING						
SD554-94*	14	±4	10	—	$385	2.2×2.6×0.4-IN. MODULE
DS340-94*	14	±4	—	1.6	$400	2.6×3.1×0.8-IN. MODULE
KINETIC SYSTEMS						
3562*	4 TO 10	±30	69.4	—	$3000	4 CHANNELS, 1 TRACKING CONVERTER PER CHANNEL; DOUBLE-WIDTH CAMAC MODULE
3395†	16	±4	—	1.0	$4250	3-CHANNEL, DOUBLE-WIDTH CAMAC MODULE
NATEL ENGINEERING						
HSRD1006*	16	±1.3	10 (14 BITS)	—	$595	SINGLE 5V SUPPLY; INTERNAL REFERENCE SYNTHESIZER; 36-PIN HYBRID
HDSR2056†	16	±1	—	0.024	$395	36-PIN HYBRID; 0.03% RADIUS ACCURACY
HDR2406†	16	±1	—	0.024	$230	1-IN^2, 28-PIN HYBRID; 0.03% RADIUS ACCURACY
TRANSMAGNETICS						
1663*	18	±0.33	1.0	—	$1600	3.1×4.6×0.82-IN. MODULE
1512*	16	±0.3	2.9	—	$880	2-SPEED CONVERTER; 3.1×5.6×0.82-IN. MODULE
1673†	14	±4	—	1.5	$540	2.6×3.1×0.82-IN. MODULE; 0.03% RADIUS ACCURACY
VERNITECH						
VSDH-409*	14	±4	10	—	FROM $500	2.6×3.1×0.82-IN. MODULE

NOTE:
MODELS ARE COMMERCIAL OR INDUSTRIAL TYPES.

KEY:
* = SYNCHRO/RESOLVER-TO-DIGITAL CONVERTER
† = DIGITAL-TO-SYNCHRO/RESOLVER CONVERTER
— = NOT APPLICABLE

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multiplying D/A converters—the sine and cosine multipliers—that are similar to those used in S/R-to-digital converters. These D/A converters cause the digital input to attenuate an ac reference signal according to sine and cosine functions, and the resulting outputs form the DSRC sine and cosine outputs—after conditioning by two power amplifiers and a Scott-T or an isolation transformer. DSRCs interface digital systems to synchro or resolver control systems.

Recent DSRC products from Natel Engineering include the 14-bit HDSR2514 and the 16-bit HDSR2056. Both feature a scale-factor variation of 0.03% max, meaning that if you use the sine and cosine outputs to generate a circle on a CRT, the circle's radius will be almost constant. This performance suits the converters for use in generating the rotating sweep in plan-position indicators (PPIs).

ILC Data Device Corp offers the 16-bit hybrid DSC-11520, which is also suitable for PPI displays (0.05% max scale-factor variation). The company's hybrid, 16-bit DRC-10520 offers 2-VA output-drive capability; it can drive a control transformer directly, without external power amplifiers. From Transmagnetics, the 1673 Series DSRC modules feature a 14-bit resolution, a 1.5-VA output drive, and a scale-factor variation of 0.03% max.

Within its Camac-compatible (computer-automated measurement and control; a standard of European origin) line of data-acquisition products, Kinetic Systems offers the Model 3395 DSRC in a double-width module. Model 3395 is a 3-channel unit that includes three 16-bit converters and associated electronics. The company also offers the Model 3562 2- or 4-channel synchro-to-digital converter, in which the resolution is pin programmable from 4 to 10 bits. This product also comes in a double-width module.

Future conversion products for synchros and resolvers promise further reductions in size and cost, as vendors introduce custom chips of increasing complexity. Second-generation CMOS chips being developed by hybrid manufacturers Analog Devices, ILC Data Device Corp, and Natel Engineering will offer improved sine and cosine multipliers along with other functions. Accelerating this trend, at least one company is working on a single-chip resolver-to-digital converter.

For the immediate future, October 29 should signal the inauguration of more uniform product quality and better discipline in the military-hybrid industry. On that day the Defense Electronics Supply Center (DESC) was expected, as of this writing, to activate a requirement for so-called custom hybrid microcircuits (the DESC labels as "custom" all hybrids not covered by a QPL slash sheet). The new rule designates that any hybrid marked or represented as compliant with MIL-STD-883 must be built in a facility certified to the new MIL-STD-1772 standard, and it must meet all the requirements of MIL-STD-38510, Appendix G.

The DESC's action has triggered a scramble for approval among hybrid manufacturers. As of this past September, 11 companies were certified and working on qualification; two more—one of them ILC Data Device—have achieved both levels of approval. According to the rules, however, all 13 companies are now eligible to supply hybrids screened per MIL-STD-883. These 13 include the S/R-converter manufacturers Analog Devices and Natel Engineering. **EDN**

For more information . . .

For more information on the S/R converters described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Analog Devices Inc
2 Technology Way
Norwood, MA 02062
(617) 329-4700
Circle No 701

Autotech Corp
343 Saint Paul Blvd
Carol Stream, IL 60188
(312) 668-3900
Circle No 702

Computer Conversions Corp
6 Dunton Ct
East Northport, NY 11731
(516) 261-3300
Circle No 703

Control Sciences Inc
9509 Vassar Ave
Chatsworth, CA 91311
(818) 709-5510
Circle No 704

ILC Data Device Corp
105 Wilbur Pl
Bohemia, NY 11716
(516) 567-5600
Circle No 705

Interface Engineering Inc
386 Lindelof Ave
Stoughton, MA 02072
(617) 344-7383
Circle No 706

Kinetic Systems Corp
11 Maryknoll Dr
Lockport, IL 60441
(815) 838-0005
Circle No 707

Natel Engineering Co Inc
4550 Runway St
Simi Valley, CA 93063
(805) 581-3950
Circle No 708

Transmagnetics Inc
210 Adams Blvd
Farmingdale, NY 11735
(516) 293-3100
Circle No 709

Vernitech
Div of Vernitron Corp
300 Marcus Blvd
Deer Park, NY 11729
(516) 586-5100
Circle No 710

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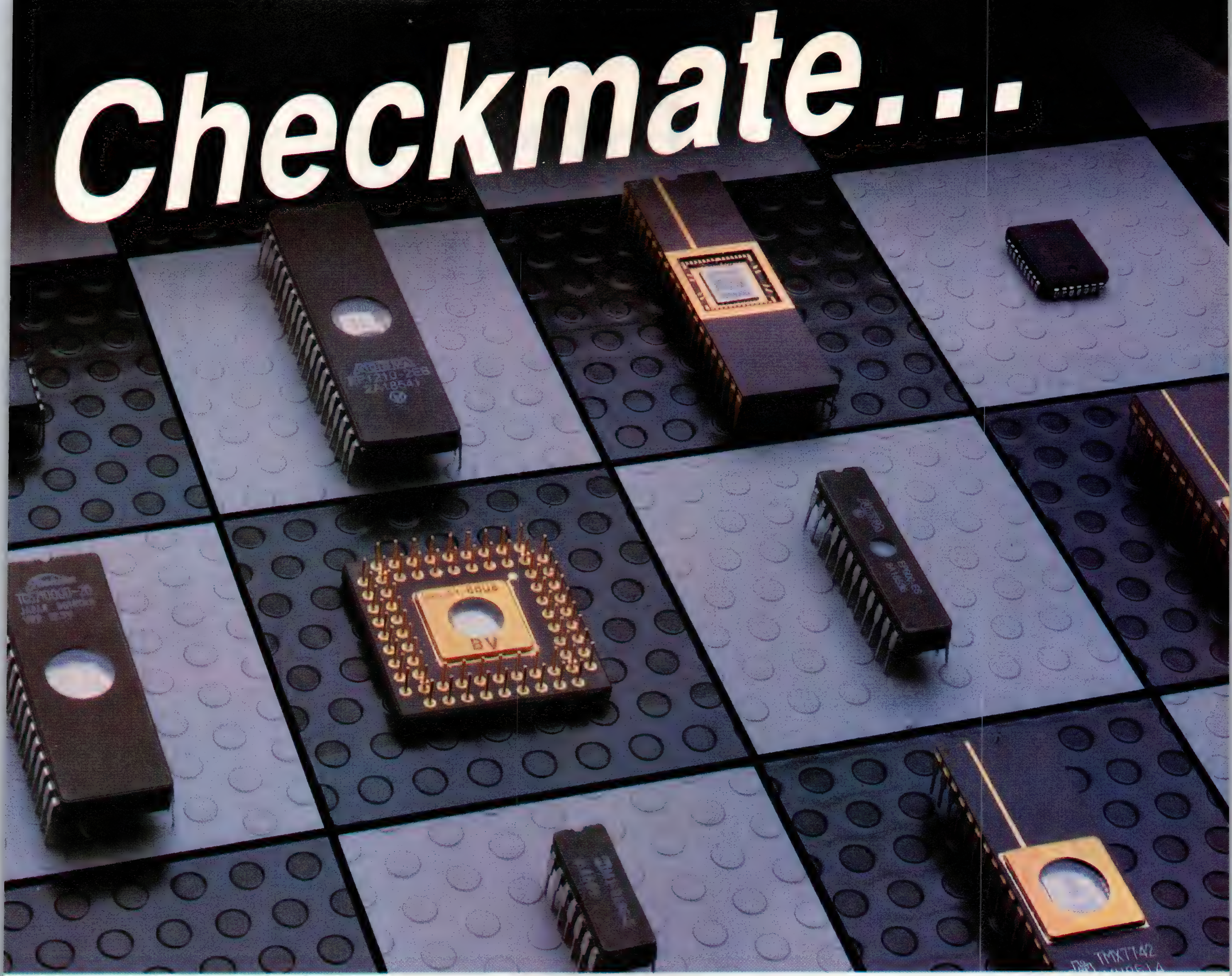
(Circle One)
High 500 Medium 501 Low 502



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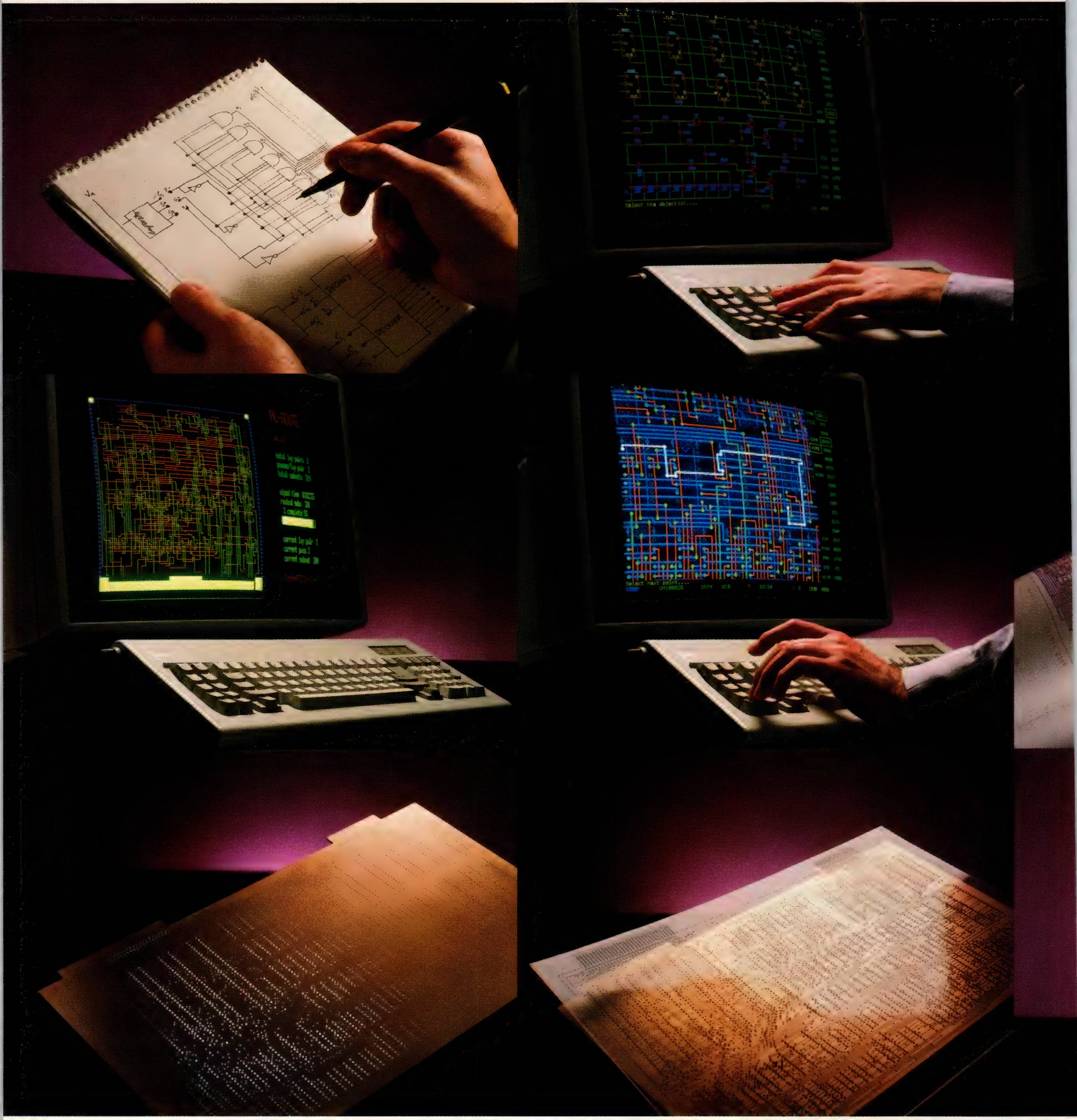

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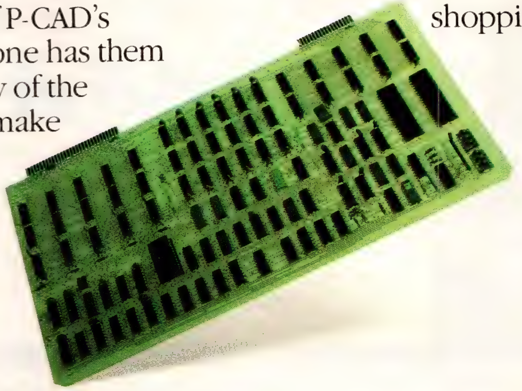

- All software runs under MS-DOS.™
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- PC-PLACE lets user define multiple placement lattices, provides tools for locating, analyzing, and optimizing the resulting placement, and handles both DIPs and discrete components.
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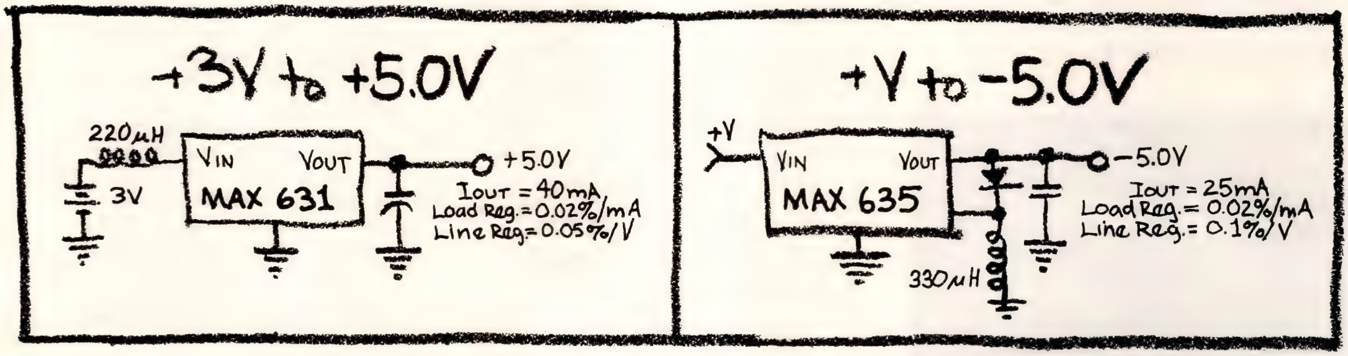
ANY VOLTAGE IN. ANY VOLTAGE OUT.



Maxim's family of CMOS DC-DC power converters can handle any input and generate any regulated output voltage (up to 100mA out or several amps with an external MOSFET).

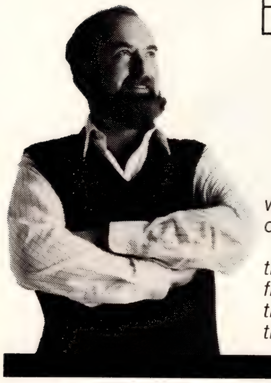
They don't need potentiometers, because the outputs are pretrimmed to the most frequently used voltages (5V, 12V and 15V). And instead of complex transformer circuitry, an inexpensive off-the-shelf coil will do. What's more, with 80% efficiency and 90μA quiescent current, they're perfect for battery-powered applications.

Now that you're converted, simply call your Maxim representative or distributor for samples and datasheets.

Maxim Integrated Products, 510 N. Pastoria Avenue, Sunnyvale, CA 94086, (408) 737-7600.

Maxim DC-DC Converters

DEVICE	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS	PRICE (100 up)
STEP UP CONVERTERS				
MAX630	2.0V to 16.5V	Vout > Vin	Programmable O/P, precision ref.	$3.20
MAX631	2.0V to 5.6V	+5V	Only 2 external components	$3.50
MAX632	2.0V to 12.6V	+12V	Only 2 external components	$3.50
MAX633	2.0V to 15.6V	+15V	Only 2 external components	$3.50
MAX641	2.0V to 5.6V	+5V	10 Watts w/external MOSFET	$3.72
MAX642	2.0V to 12.6V	+12V	10 Watts w/external MOSFET	$3.72
MAX643	2.0V to 15.6V	+15V	10 Watts w/external MOSFET	$3.72
MAX4193	2.4V to 16.5V	Vout > Vin	Programmable output	$2.15
INVERTING CONVERTERS				
MAX634	3.0V to 16.5V	up to −20V	Programmable O/P, precision ref.	$2.90
MAX635	3.0V to 16.5V	−5V	Only 3 external components	$3.50
MAX636	3.0V to 16.5V	−12V	Only 3 external components	$3.50
MAX637	3.0V to 16.5V	−15V	Only 3 external components	$3.50
MAX4391	4.0V to 16.5V	up to −20V	Programmable output	$2.70
STEP DOWN CONVERTERS				
MAX638	3.0V to 16.5V	Vout < Vin	Only 3 external components	$3.50



MAXIM

Maxim's family of DC-DC converters was developed under the direction of Maxim co-founder and VP of R&D, Dave Fullagar.

At Fairchild, back when giants walked the earth, Dave helped pioneer the world's first linear ICs. And he personally designed the most successful op amp ever built, the μA741.

What's more, as Intersil's first engineering director, he was responsible for the emergence of CMOS as the standard technology for analog ICs.

Add to all that the fact that Dave is 6′3.″ And I guess you could say that Dave is a giant in the annals of analog IC technology.

Whatever an annal is.

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Accelerator boards boost speed of PCs and achieve performance comparable to PC/ATs

Chris Terry, *Associate Editor*

If you're using an IBM PC, PC/XT, or compatible machine to run applications that perform extensive calculations (such as large spreadsheets) or generate complex graphics (such as Autocad), you're probably weary of waiting interminably for each operation to complete before you can go on to the next. If you really need the speed of a PC/AT and all of its features, you'd be well advised to go buy one—or one of its even faster clones. But if your budget won't allow you to buy a PC/AT, you can still make your PC or PC/XT run a good deal faster by installing one of the many accelerator boards currently available at prices from $100 to $995.

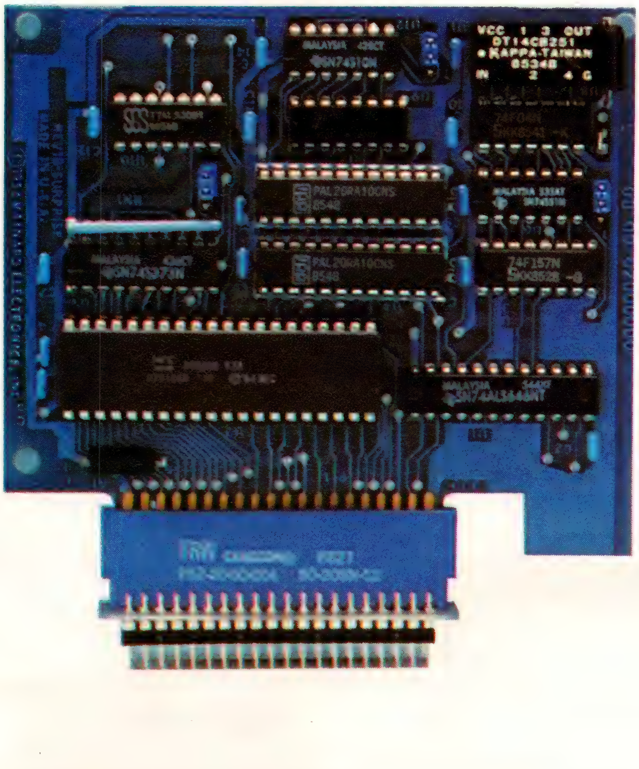
These boards fall into two main categories: those that replace the 8088 CPU with a faster 8088, 8086, or NEC V20 chip and that don't need an expansion slot; and those that retain the 8088 for I/O processing but that use an expansion slot to add an 80186 or 80286 CPU chip and fast memory to run the software.

Your main problem will be to choose the accelerator that will suit you best—and the decision won't be easy. You may run into installation problems, software compatibility problems, or both. When installation is complete, you still won't have a real PC/AT, but you'll find that most (but probably not all) of your software runs considerably faster than it did before you modified your machine. You'll notice the most improvement in performance in computation-intensive applications—spreadsheets and graphics (and games). You'll see little or no improvement in disk- and I/O-intensive applications such as word processing because, although the software will run faster than before, the disk or I/O device won't.

Replacement accelerators rely on the premise that most components of the IBM PC, PC/XT, and clones will operate perfectly well at clock speeds somewhat higher than those specified by IBM. For example, in the PC, the 8088 CPU chip runs at 4.77 MHz, but Intel rates it at 5 MHz. In fact, most 8088 chips will perform properly at clock speeds as fast as 6.5 MHz, and a few can operate at more than 7 MHz. The same applies to the 8087 math coprocessor chip, although this chip is a little more exacting than the 8088. The IBM bus, too, has electrical characteristics that permit data transfers over the bus at rates approaching 10 MHz, provided that the sending and receiving chips can also operate properly at these speeds.

Speeding up PC operation, however, involves more than just replacing the standard master-oscillator crystal with one of higher frequency. The 8224 clock chip uses a 14.31818-MHz crystal to generate not only the 4.77-MHz CLK88 clock signal for the CPU but also the 2.38-MHz PCLK signal and the 3.578-MHz OSC signal. The 8253 counter-timer chip on the mother board uses the PCLK signal to generate periodic interrupt requests that drive the system's software clock/calendar; the IBM color graphics adapter (CGA) board uses the OSC signal to generate the color and sync signals required by color monitors.

Thus, if you want to speed up the CPU clock, you'll have to replace the 8224 clock chip with circuitry that not only generates a faster CPU clock but maintains the standard frequencies of the PCLK and OSC signals; otherwise, the system won't keep proper time, and you



You can more than double a PC's speed *without taking up an expansion slot when you use an accelerator like this $249 version from Maynard Electronics. A mounting kit that adapts the accelerator to some IBM PC compatibles costs $30.*

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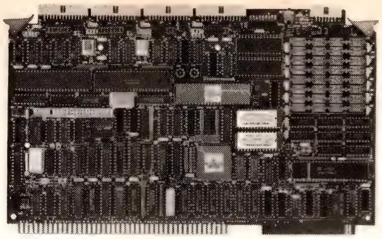

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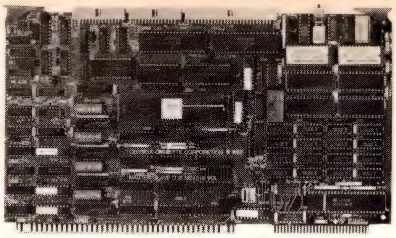

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- A triple 16-bit timer/counter
- (7) prioritized-vectored interrupts
- Omnibyte two year limited warranty

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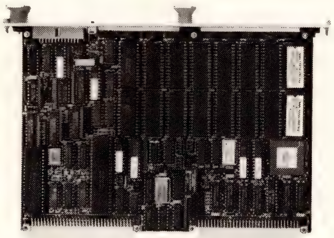

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- (8) pairs of 28-pin sockets for RAM and ROM (up to 448K RAM or 896K ROM)
- (2) RS-232C serial ports using (1) 68681 DUART
- (2) 8-bit parallel I/O ports using (1) 68230 PI / T
- System controller functions are supported
- (7) Prioritized bus or auto vectored prioritized interrupts
- Omnibyte two year limited warranty

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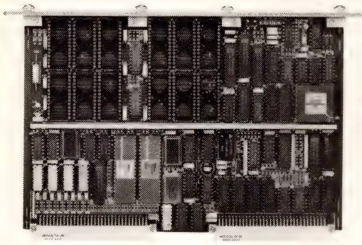

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- (3) 16-bit timer/counters (in Z8536)
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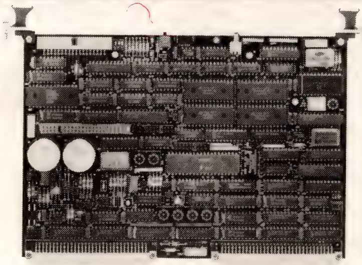

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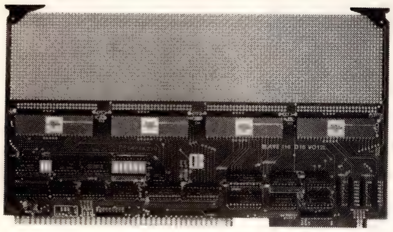

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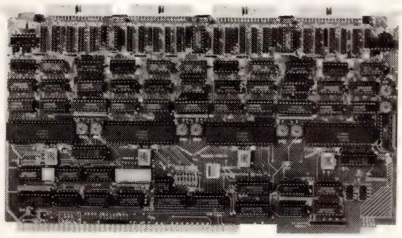

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- (4) 68681 DUART chips
- (4) Multi-function programmable 16-bit counter/timers
- Omnibyte two year limited warranty

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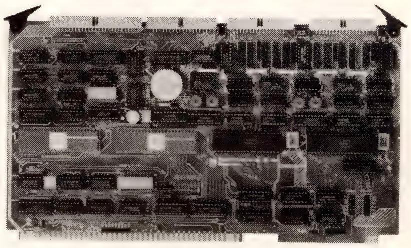

0B68K/INT(S)™ MULTIBUS HOST ADAPTER/ SERIAL I/O BOARD

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- (2) 68681 DUART chips
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- Parallel printer port
- Real time calendar clock with battery back-up
- Omnibyte two year limited warranty

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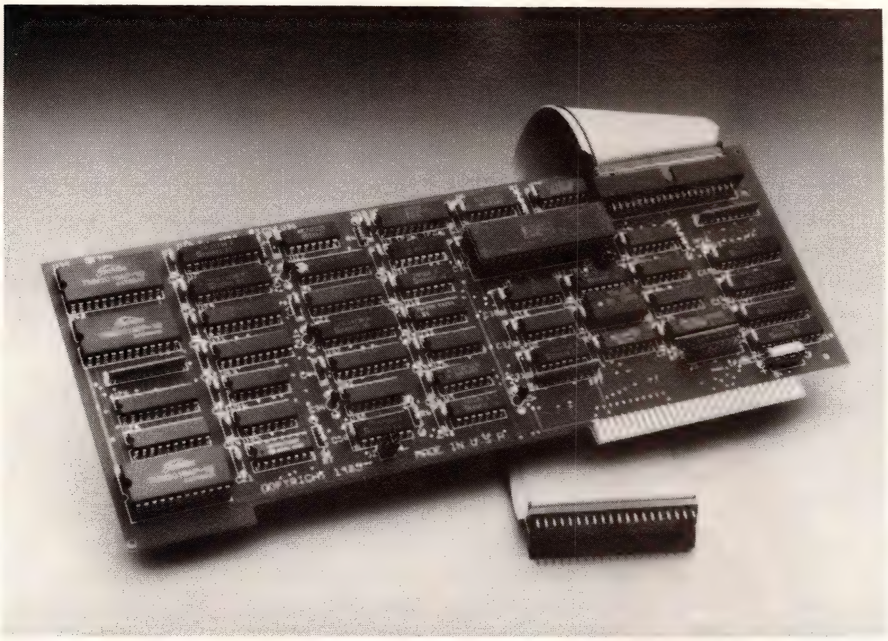

The Quadsprint, typical of coprocessor accelerators, *uses an 8-MHz 8086 and cache memory to achieve its high performance.*

won't be able to use a CGA board. To obtain a significant improvement in performance, you'll also need to replace the 5-MHz 8088 with an 8-MHz 8088-2 or a NEC V20-8 (which is an equivalent of the 8088-2).

Each of the accelerators in the replacement category consists of a piggyback card that either plugs directly into the 8088 socket or connects to it via a ribbon cable and header. Likewise, the accelerator provides a ribbon cable and header that plugs into the 8224 socket. If you have one of the older PCs, in which the 8224 is soldered directly to the mother board, you'll have to clip the leads of the 8224, unsolder the remnants of the leads, and install a socket (usually provided by the vendor) in place of the 8224.

Speed obtainable is limited

CPU replacement is the simplest and least expensive approach to accelerating a PC, and has the advantage that only the clock circuits are modified. You don't have to reconfigure the system in any way, and there are no additional devices that might need software drivers or use I/O ports that could conflict with your standard peripherals. Nevertheless, you may still encounter a few problems.

The 8087 math coprocessor is one possible source of trouble. The standard 8087 is rated for 5 MHz and, although some chips may run at speeds as high as 6.1 MHz, you'll probably have to install the 8-MHz 8087-2 if you want to run your CPU at more than 7 MHz. Also, even the most recently introduced versions of Nucleus's Overthruster ($195) won't run at more than 4.77 MHz if you have an 8087 in your system. The same holds true of recent versions of Dynatec Systems' Supercharger ($279): They won't even boot the system in the presence of an 8087. If you're considering either of these boards, both of which perform well in all other respects, check with the manufacturers to see that the problem has been eliminated (which may well be the case by the time this article appears in print).

Your system memory may also place some constraint on the speed increase you can obtain. RAM chips rated for 250-nsec access times can run at 6.1 MHz, but for faster clock speeds you'll probably have to install RAM chips that have access times of 200, 150, or even 120 nsec. These chips aren't expensive, but older PCs may have the first bank of chips soldered to the mother board —removing them and installing sockets for faster chips is a delicate, time-consuming, and frustrating operation.

The ROM chips that contain the BIOS firmware can also limit the speed at which your PC will run. In most PCs you can read the ROM properly at clock speeds as fast as 6 MHz, but beyond that limit the system won't work.

Two solutions are at hand

You have a choice of two ways of circumventing this problem. Some boards (for example, the Supercharger) clock the CPU at a fixed high speed but monitor the chip-select lines of the ROM and of the DMA controller (which is rated at 5 MHz); when the system initiates an access to either of these devices, the accelerator circuitry temporarily drops the clock speed back to 4.77 MHz, or inserts wait states, to ensure correct operation of the device.

Other accelerators, such as Microspeed's Fast88 ($149), don't attempt to adjust the operation for ROM or DMA accesses but instead provide three or four switch-selectable clock speeds. By trial and error, you arrive at the fastest speed at which your system operates correctly. After booting the system at the standard speed, you can manually switch to the higher speed.

Speed can kill

Software that has built-in timing loops may also present a problem because the higher clock speed reduces the time required for one pass through the loop. Some communications software (and some games—especially the shoot-'em-down kind) may produce unexpected results or may not work at all at the higher clock speeds. Fortunately, communications programs that use timing loops to wait for dial tones or to pause between sections of a dialing string usually have an installation menu that allows you to specify your clock speed.

You may also find that some copy-protected software is speed-sensitive. You'll almost certainly have to start copy-protected programs at the standard speed, but many will run properly if you switch to a higher speed after the program is loaded.

The replacement accelerators have simplicity as their virtue, and they deliver a modest but reliable increase in performance. There is, however, a limit to that increase because the PC is designed as an 8-bit machine, even though the 8088 operates internally on 16 bits at a time.

If you want throughput that actually approaches or exceeds that of the PC/AT, you need a CPU chip that not only accepts a faster clock but also uses fewer clock cycles to execute any given instruction. The 80186 and 80286 meet these requirements, and designers have used both to drive coprocessor accelerators (although the 80186 is now overshadowed by the faster, more versatile 80286 that's used in the PC/AT).

Cache memory supplies 8k bytes

All of the available coprocessor accelerators provide a fast, 16-bit CPU that runs at clock speeds between 8 and 12 MHz. Accelerators that fit into a half-card slot generally have a cache memory of 4k to 8k bytes (for instance, Victor Technologies' $595 SpeedPac 286 and Orchid's $695 TinyTurbo 286); they access the PC's own memory via the 8-bit bus and bring code and data into the cache for high-speed processing. To allow you to revert to standard 8088 operation at 4.77 MHz, you have to transfer the 8088 to a socket on the accelerator; a ribbon cable and header connect the accelerator to the original 8088 socket on the mother board. These cards also have a socket for an 80287 math coprocessor. Quadram's $395 Quadsprint is also in this class, but it occupies a full-length card slot.

Generally, coprocessor accelerators that fit into a full-length slot come with a full complement of fast 16-bit memory; when the accelerator's in the fast mode, the 16-bit memory replaces the PC's memory. Fast memory capacity ranges from 640k bytes (Classic Technology's $995 286 Speed Pak) to 1M bytes (Applied Reasoning Corp's $1195 PC-Elevator, Phoenix Computer Products Corp's $1495 Pfaster, and Orchid's $1195 PC-Turbo-286e). These and similar cards allow you to expand the 16-bit memory to as much as 2M bytes, either by means of a separate long card (for example, the 286 Speed Pak offers this option), or by means of piggyback add-ons (Pfaster and PC-Turbo-286e allow you this option).

Watch out for snags

Installing a coprocessor accelerator is generally not quite as simple as installing a replacement accelerator. You may have to disable all 8-bit

Check the reviews

Before making a final decision on which accelerator will suit you best, you should check some of the reviews that have appeared during the last 12 months. In November 1985, *PC Magazine* reviewed and benchmarked six accelerator boards and seven high-performance PC- and PC/AT-compatible computers **(Ref 1)**. In September 1986, it published in-depth reviews of five replacement accelerators **(Ref 2)** and 14 coprocessor accelerators **(Ref 3)**; these articles are required reading if you want to understand not only the technical requirements of a good accelerator but also the quality of documentation supplied with each item reviewed and the problems you may encounter in installing and using the boards.

Most recently, the reviews in *Dr Dobb's Journal* describe benchmark tests of the IBM PC, PC/AT, and six accelerator boards **(Ref 4)**. An article in *PC Week* provides case histories and users' experiences that may be of interest **(Ref 5)**, but this article has fewer technical details than the other articles cited.

Both *PC Magazine* and *Dr Dobb's Journal* found that Peter Norton's Sysinfo program, though widely used as a comparative measure of performance, gives somewhat inconsistent results. For this reason *PC Magazine* did not use the program at all, but substituted benchmark tests that are more representative of the results you can expect in running a wide variety of applications. *Dr Dobb's Journal* used Sysinfo, but supplemented it with compilation and linking of a 400-line C program, the Sieve of Eratosthenes, and the Dhrystone benchmark tests.

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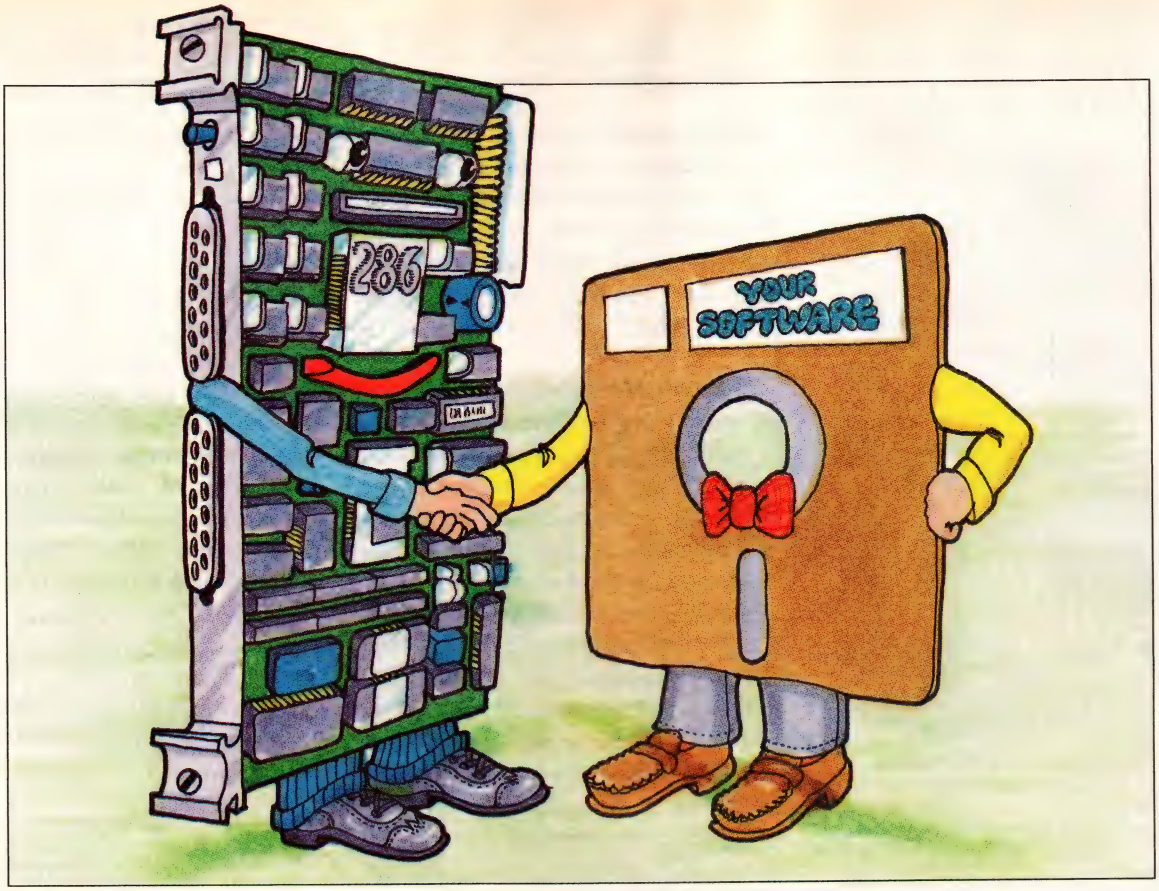
1. "Breaking the Speed Limit," *PC Magazine*, November 12, 1985, pg 130.
2. Davis, Stephen, "The No-Slot Alternative to Acceleration (and Why It Makes Sense)," *PC Magazine*, September 16, 1986, pg 169.
3. Petzold, Charles, "Accelerator Boards—Power for a Price," *PC Magazine*, September 16, 1986, pg 125.
4. Elkins, Mike and Steve King, "High-Speed Thrills," *Dr. Dobb's Journal of Small System Tools*, September 1986, pg 86.
5. Cummings, Steve, "Accelerator Cards," *PC Week*, July 8, 1986, pg S/3.



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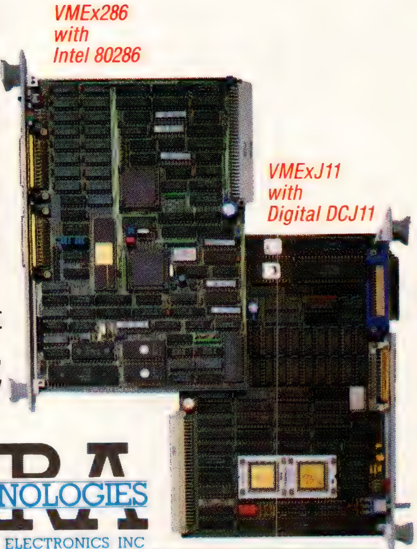

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memory except the first 256k bytes, or at least any expansion memory that would conflict with memory on the accelerator card. You'll certainly have to install some software, and perhaps modify your AUTOEXEC.BAT and CONFIG.SYS files.

If you're considering an accelerator with a large memory, you'll have to check to see how the board manages it. Some accelerators have only expanded conventional memory (ECM) that's switched in 64k-byte banks and may not meet your needs; others are compatible with the LIM (Lotus/Intel/Microsoft) extended memory specifications (EMS). You should pick a board that's LIM compatible if you're going to run very large spreadsheets, for example, or programs that use EGA graphics.

Furthermore, if you're proposing to run EGA graphics, check that the latest version of the card of your choice is EGA compatible: Early versions of some accelerators were either incompatible with EGA or had bugs in that area that proved troublesome. Probably your best choice would be Orchid's $945 TurboEGA, which combines an 80286 accelerator and an enhanced graphics adapter on one board. This board paints complex full-screen images so fast that when you first see it you think you're watching a beefed-up Sun or Apollo. Also, for text displays, the TurboEGA's 80286 accesses the ROM BIOS in 16-bit words rather than in bytes, thus allowing it to update the screen at a gallop. And, for good measure, this board is capable of emulating three other graphics cards: IBM's monochrome adapter, IBM's color graphics adapter, and Hercules' graphics card. **EDN**

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For more information . . .

For more information on the accelerator boards described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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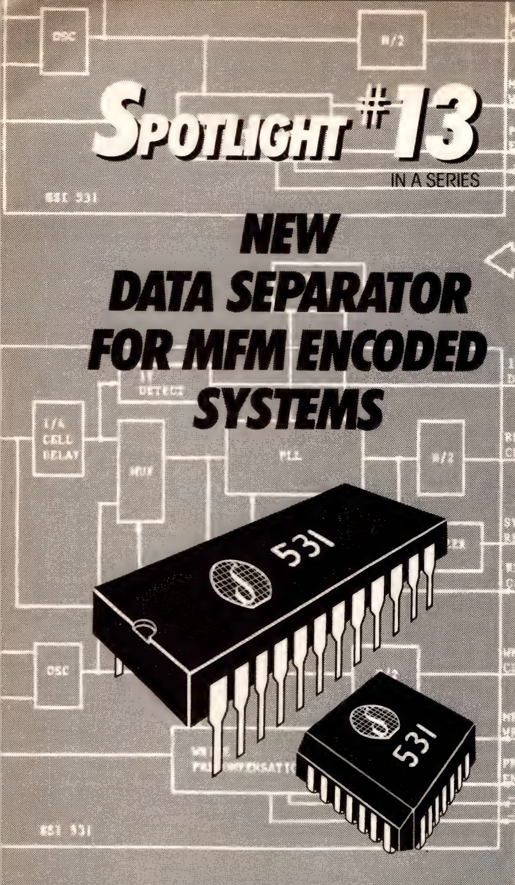

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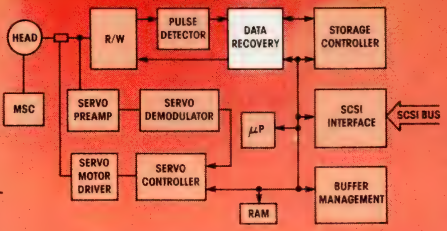

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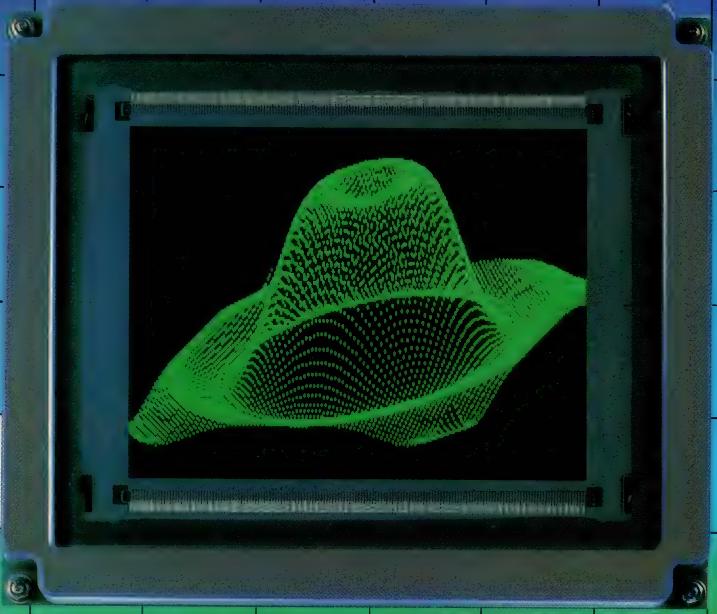
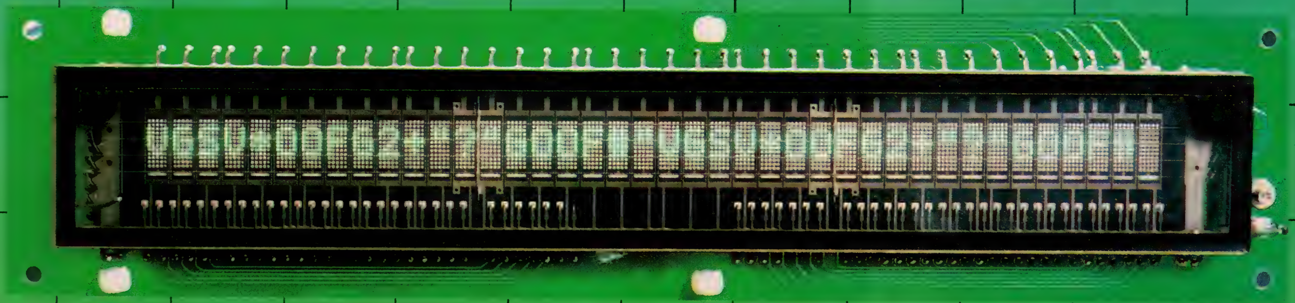


Graphic Module



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GP1009	240 × 64	0,45	107,9 × 28,7	VFD	40 × 6
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M40SD02CA	40 × 1	5 × 7 dot w/cursor	3.5 × 5.0	222
M40SD42CA	40 × 1	5 × 12 dot w/cursor	3.5 × 8.75	222
M202SD03CA	20 × 2	5 × 7 dot w/cursor	3.5 × 5.0	222
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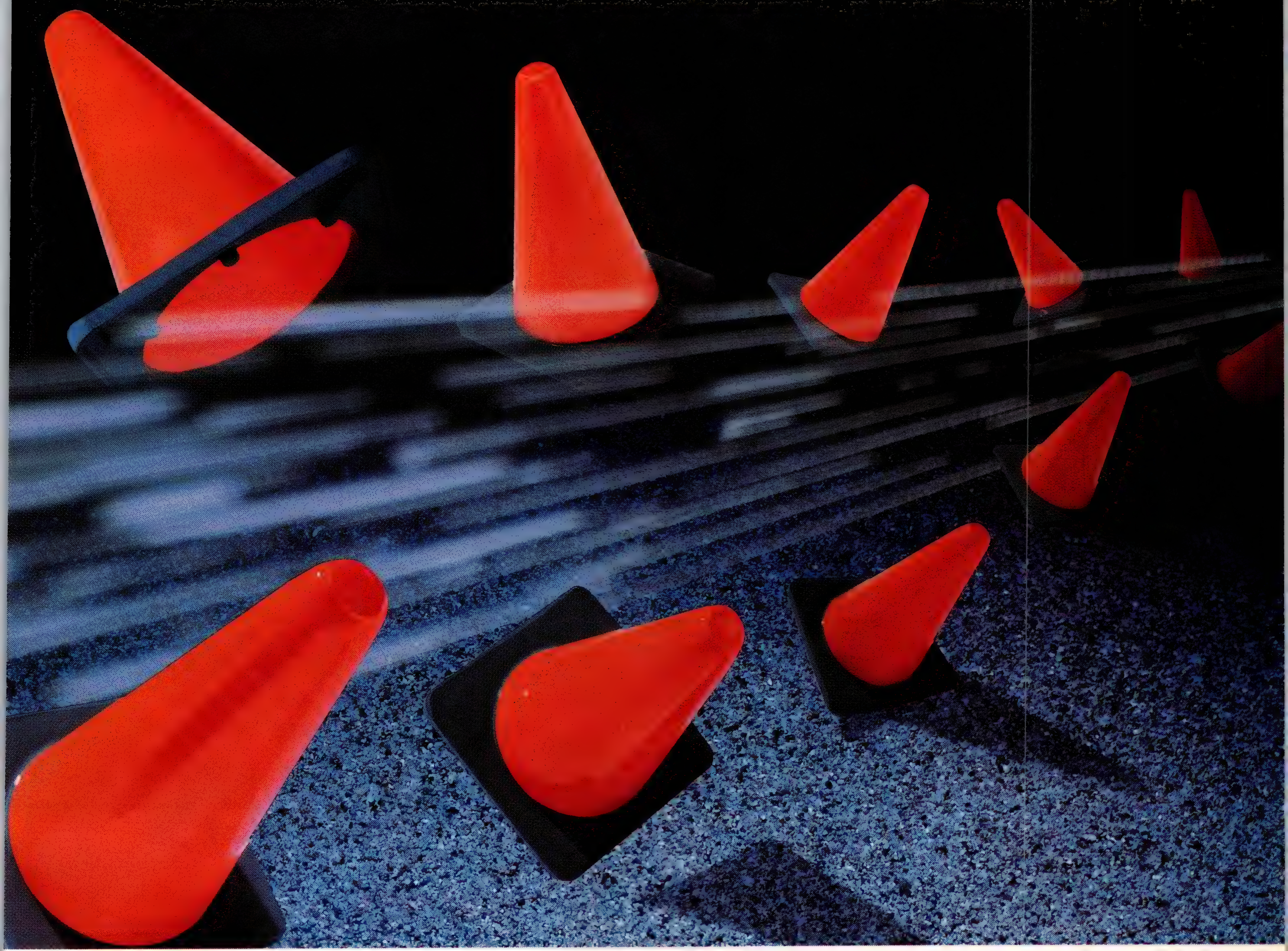

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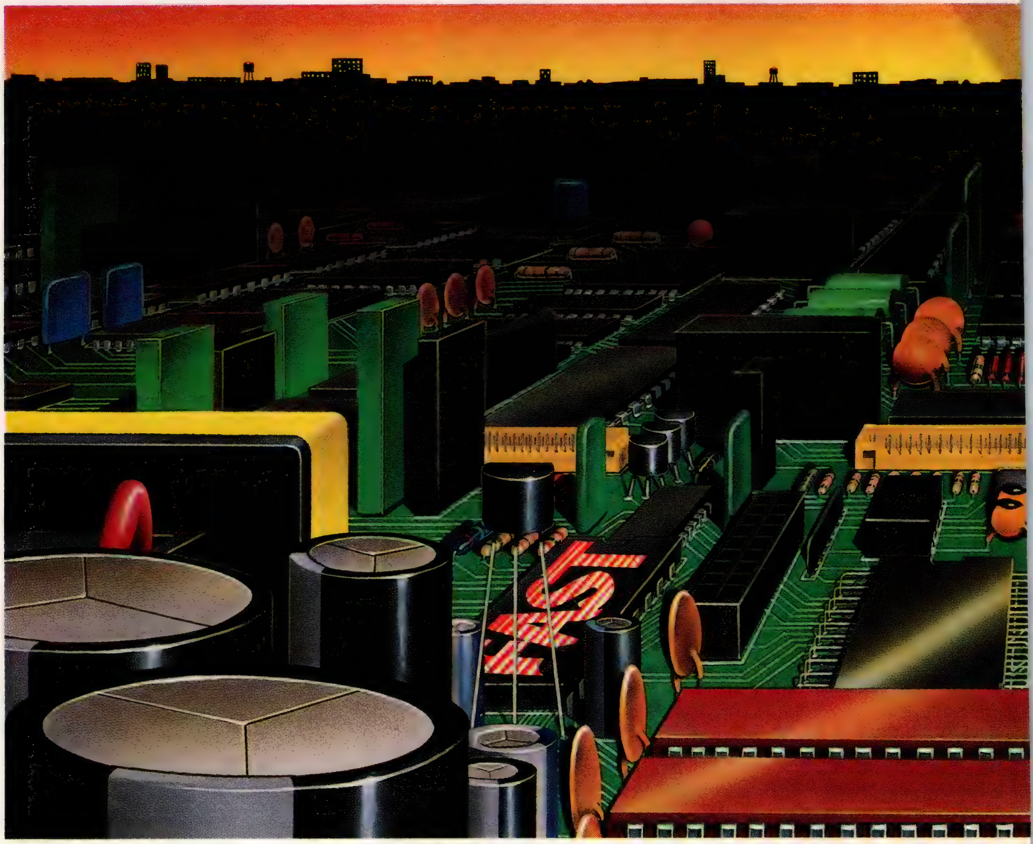

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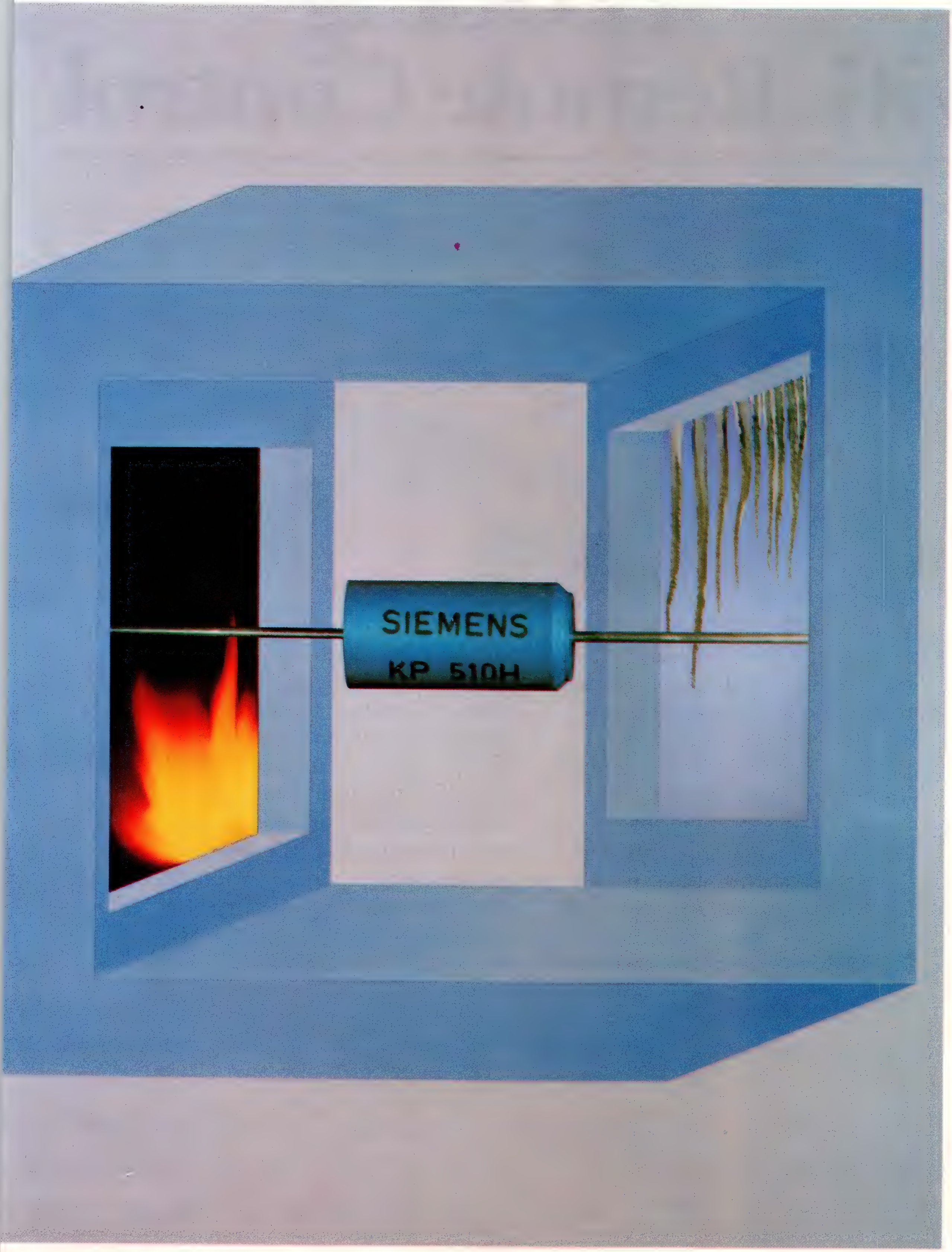

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The µPD612X Series

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Remote control is the name of the game when it comes to quick and efficient manipulation of audio-visual equipment and other home or office appliances. And NEC's new CMOS-based µPD6124/5/6 Series is the infrared remote control transmitter that combines programmability with small packaging and low power consumption. Excellent performance stems from a 1024 x 10 bits program memory, 32 x 4 bits data memory, and a large instruction set. A standby mode plus low operating voltage reduces battery design to a minor detail.

TYPE	KEYS	PACKAGE
µPD 6124	32	20 PIN MINIFLAT
µPD 6125	64	24 PIN MINIFLAT OR SLIM DIP
µPD 6126	96	28 PIN MINIFLAT

The µPD612X Series features 32, 64 or 96 key inputs. All remote control commands and functions are programmable and the transmission format can be customized. The operating frequency is either 38 or 58 KHz.

West Germany: Düsseldorf 02 11/65 03 01, Telex 8 58 996-0
The Netherlands: Eindhoven 0 40/44 58 45, Telex 51 923
France: Paris 01/39 46 96 17, Télex 699 499
Italy: Milano 02/67 09 108, Telex 315 355
Sweden: Täby 08/73 28 200, Telex 13 839
UK: Milton Keyes 09 08/69 11 33, Telex 777 565

NEC

CIRCLE NO 5

Electronica 86 conferences cover topics from VLSI devices to power semiconductors

Peter Harold, *European Editor*

Electronica 86, which takes place November 11 to 15 in Munich, West Germany, provides not only an opportunity to survey new product offerings in the electronic-component and -assemblies market, but also an opportunity to attend four technical conferences. The 12th International Conference on Microelectronics, the 3rd International Macroelectronics Conference, the Symposium on Quality Assurance, and a technical conference devoted to the hardware/software tradeoffs involved in digital signal processing all run in conjunction with the exhibition. This year, all the conference sessions will feature a simultaneous German/English translation service.

The microelectronics conference, which takes place on the afternoon of November 10 and throughout the day on November 11, intersperses contributed papers between lectures from invited speakers. The conference focuses on VLSI devices, including standard and application-specific ICs (ASICs), the application of VLSI devices to digital signal processing, advances in bipolar VLSI technologies and the likely competition between bipolar and MOS, and new surface-mount packaging concepts for devices having high pin counts. Papers on gallium-arsenide technology, alternative silicon-based technologies, and bionics will attempt to predict the market impact of these technologies in the 1990s and beyond.

Divided into four sessions, the macroelectronics conference on November 13 addresses power semiconductor devices. The first session examines smart-power devices, which incorporate digital control and feedback to improve the performance and reliability of their power-switching elements. The two sessions that follow examine new bipolar and field-effect power transistors and GTO thyristors. The session on thyristors includes a paper that compares GTO thyristors with power transistors. Rounding out the conference is a session on static power converters; this talk focuses on the problem of preventing the converters' pulsed input current waveforms from affecting their line supplies.

All about DSP

If you're interested in digital signal processing, you'll want to attend the Sensorik conference, which takes place on the morning of November 14. Its technical sessions will examine all aspects of digitizing analog signals and processing them in the digital domain. The conference will focus particularly on the hardware and software tradeoffs you can make when you design a DSP system. It will also provide an explanation of the basic mathematics involved in DSP algorithms.

The 1-day symposium on quality assurance, which is slated for November 12, will highlight the need for component manufacturers, equipment manufacturers, and users to cooperate in assessing product quality. Topics for discussion include the definition of requirements, defect and failure analysis, corrective procedures, manufacturing process changes, and documentation methods.

If you wish to attend any of these conference events, you need to register in person at the conference office as soon as you get to the exhibition. The conference fees, which range from DM 140 to DM 340 depending on the conference and the number of sessions you attend, include admission to Electronica 86 on all five days of the exhibition. The fee for admission to just the trade fair ranges from DM 35 to DM 85, depending on the number of days you attend.

Could be 2000 exhibitors

As for the exhibition itself, it looks set to rival the 1984 event in size. The preliminary exhibitor list prepared in May listed over 1800 registered exhibitors from around 35 countries, and the list is expected to top 2000 before the exhibition opens. As they did two years ago, exhibits will occupy all 19 of the main halls at the exhibition site. The displays are divided into a number of component and subassembly categories, so you'll find it easy to concentrate on your particular areas of interest.

On the following pages you'll find information about some of the new European product introductions that will be on display at Electronica. Designers who are considering moving to surface-mount assembly, for example, will find the exhibition a good place to locate SMD component suppliers. You'll certainly find a wide range of components, some new and some familiar, packaged for surface mounting.

The recent spate of DSP chips from both European and US vendors will also be on display, so you'll want to take the opportunity to compare the software support and emulation capabilities that DSP-chip manufacturers provide for their devices.

Many companies that don't offer standard products—particularly firms in the semicustom and service sectors of the electronics industry—will use their stands to demonstrate their capabilities. For example, Eurosil (Eching, West Germany), Mietec (Oudenaarde, Belgium), and

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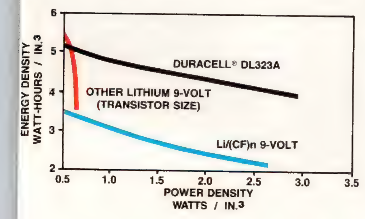

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CIRCLE NO 14

Ferranti (Oldham, UK) will all be exhibiting new capabilities in semicustom design.

Allowing you to design your own semicustom DSP devices, Eurosil is extending its gate-array macro and standard-cell libraries to include DSP-oriented functions. The new library elements include configurable fast multipliers, RAM, ROM, PLAs, ALUs, and sequencers; new elements specific to the standard-cell library include analog functions, such as comparators and A/D and D/A converters. Eurosil will exhibit in hall 23, stand 23-A-5.

Mietec will feature Made, the company's analog and digital CAE system for custom and semicustom design, in hall 19, stand 19-B-7. The VAX-based Made software allows you to design in CMOS, using single or double polysilicon and single or double metal layers, or in BIMOS, a technology that permits you to mix high-voltage bipolar and low-voltage CMOS components on the same die. The CAE package covers all aspects of the design from schematic capture to layout verification, and it includes modules for the automatic compilation of several functions, including switched-capacitor filters, PLAs, RAM, and ROM.

Ferranti, in addition to displaying its VAX-based Ulacad CAE software, will exhibit an IBM PC-based design system for the company's range of Digilin linear/digital and linear arrays. Based largely on commercially available hardware and software packages, the design system provides interactive graphics for design entry, dc and ac circuit simulation, evaluation of noise sensitivity, and Fourier analysis. A circuit library provides macros for defining active components such as op amps, comparators, and current sources. The basic component parameters provided for the company's digital/linear and linear arrays suit component-level design. You'll find Ferranti in hall 24, stand 24-A-6.

Among the hybrid manufacturers, Thomson Hybrid ICs, a division of Thomson Semiconductors (Paris, France), will exhibit a building-block approach to the design of power hybrids (hall 24, stand 24-B-10). Using copper packaging, BeO or AIN substrate materials, and brazed components, the company can produce hybrids having power-dissipation specs as high as 200W and current and voltage ratings to 50A and 1500V. You can design a semicustom power hybrid by using a library of 12 electronic subfunctions, such as rectifiers and regulators, and 6 package options.

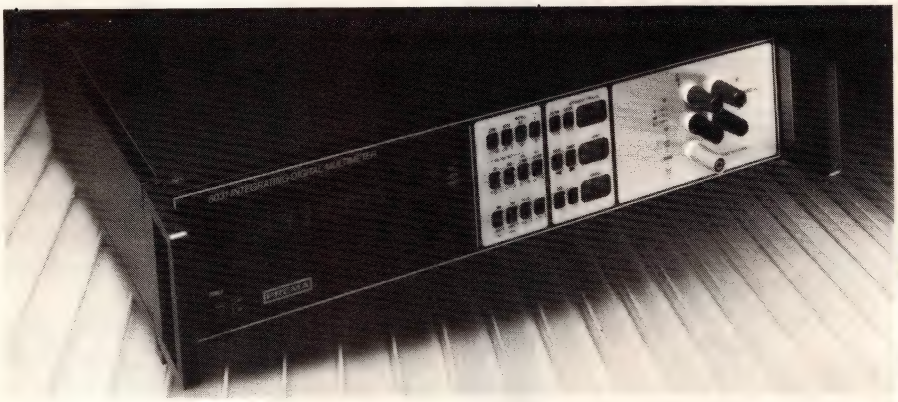
3-D hybrid technology covered

In addition, the company will display its 3-dimensional hybrid technology. Targeted for high-speed, high-density digital hybrids, this technology allows you to integrate resistors and capacitors into the subsurface layers of the hybrid's interconnecting structure to create 3-dimensional internal structures, such as cavities, vias, and walls. It also allows you to mount various types of chip packages and naked dies. The process uses a low-dielectric-constant ceramic substrate and low-resistivity conductor material to reduce signal-propagation delays. Theoretically, the process will allow you to design with as many as 40 interconnect layers.

Besides the companies mentioned, the exhibition will feature a number of other semicustom and hybrid manufacturers. For more information on the Electronica 86 exhibition and its associated conference program, contact Münchener Messe- und, Ausstellungsgesellschaft mbH, Messegelände, Postfach 12 10 09, D-8000 München 12, West Germany, (089) 51070, TLX 5212086. **EDN**

Article Interest Quotient
(Circle One)
High 506 Medium 507 Low 508

6½-digit DMM performs math functions and features optional 20-channel scanner



The 6031 integrating digital multimeter allows you to select an integration time in the 20-msec to 20-sec range with corresponding increases in scale length from 4½ to 6½ digits. The unit's basic 1-year dc-voltage and resistance accuracy is 0.003% (23°C ±5°C). Its maximum dc-voltage and resistance resolution specs are 100 nV and 100 μΩ.

The DMM's 5½-digit ac-voltage function measures dc- or ac-coupled true-rms values. Its maximum ac-voltage resolution is 10 μV, and its best accuracy is ±(0.07% of reading+0.05% of range) for the 2 to 200V ranges between 30 Hz and 1 kHz. The DMM measures dc or true-rms-ac current to 2A and gauges temperatures between −200 and +850°C with 0.01°C resolution.

The DMM's math functions include offset and multiplication factors, as well as the computation of ratios, powers, percentage deviations, and polynomials. You can also compute nonlinear functions, including log, square root, tangent, and arc tangent, plus a range of statistical functions. The DMM also performs limit checking and records maximum and minimum values. Its optional scanner allows you to scan as many as 20 input channels. Around DM 7000.

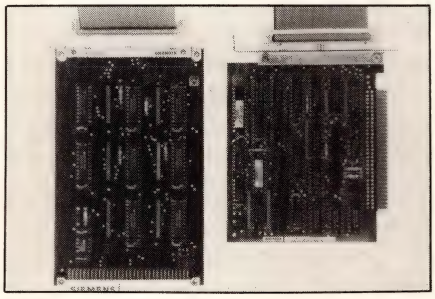
Prema GmbH, Robert-Koch-Strasse 10, 6500 Mainz 42, West Germany. Phone (06131) 50620. TLX 4187666.

Circle No 666

Prema Precision Electronics Inc, Sunset/Vine Tower, Suite 1126, 6290 Sunset Blvd, Los Angeles, CA 90028. Phone (213) 463-2294. Hall 25, Stand 25-B-11

Circle No 667

Two-card, 1.5m interface links IBM PCs to SMP Bus for industrial I/O applications



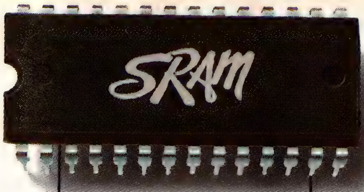
Using the the SMP-E570-A1 interface, you can control an 8-bit SMP Bus industrial I/O subsystem from an IBM PC, PC portable, PC/XT, PC/AT, or compatible computer. The interface comprises a plug-in card for the PC Bus and another for the SMP Bus. The cards are linked by a 1.5m, 50-way ribbon cable. The PC operates as the bus master for the SMP Bus system, but this arrangement doesn't prevent you from using SMP Bus intelligent I/O cards that have onboard slave CPUs.

The interface maps the SMP Bus system into 64k bytes of the PC's memory space and 256 bytes of its I/O space. The interface supports direct and memory-mapped I/O operations from the PC to the SMP Bus, and it permits the PC's DMA controller to perform DMA transfers to and from the SMP Bus system. Jumper links on the PC Bus card allow you to set 1 to 7 wait cycles for SMP Bus accesses, to set up interrupt channels, and to set the location of the SMP Bus's memory, memory-mapped I/O, and direct I/O in the PC's address map. You can also select the frequency of the SMP Bus master clock to be 1× or 0.5× the PC's clock frequency. You can interface as many as four SMP Bus systems to one PC. The SMP-E570-A1 costs DM 1875.

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025. Hall 23, Stands 23-A-4 and 23-B-4

Circle No 665

The Mitsubishi 256K *Mixed-MOS SRAM*



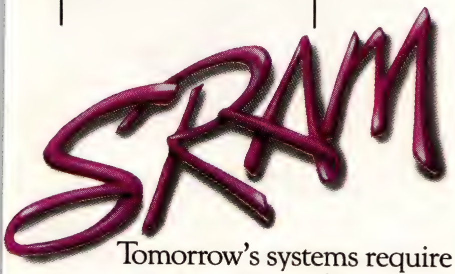
Mitsubishi Offers Fast Access For Large Memories.

Fast SRAM Product Selection Guide

Part No.	Organization	Access Time 25 ns	35 ns	45 ns	55 ns	70 ns	85 ns	100 ns	120 ns	150 ns	Package Types Plastic DIP	Leadless Chip Carrier	Small Outline Package
M5M21C67	16K x 1		•	•	•						• 20 PIN	•	
M5M21C68	4K x 4		•	•	•						• 20 PIN	•	
M5M5165	8K x 8					•		•	•	•	• 28 PIN		• 28 PIN
M5M5178*	8K x 8			•	•						• 28 PIN (300 mil wide & 600 mil wide)		• 28 PIN
M5M5179*	8K x 9			•	•						• 28 PIN (300 mil wide only)		• 28 PIN
M5M5187	64K x 1	•*	•*	•	•						• 22 PIN	•	
M5M5188**	16K x 4	•*	•*	•	•						• 22 PIN	•	
M5M5256	32K x 8					•*	•*	•	•	•	• 28 PIN		• 28 PIN

*New product offering, subject to availability.

**Also available in 24 pin version with output enable ($\overline{OE}$) function.



Tomorrow's systems require ever-increasing performance from cache, control store, buffer and program memory.

Committed to meeting these requirements, Mitsubishi's growing family of CMOS static RAMs offers a selection of organizations, densities and speeds for high performance, optimum board density and low power dissipation. Real choices, with more to come.

Now, the newest members of Mitsubishi's SRAM family, the M5M5187, M5M5188 and M5M5256, combine the advantages of resistor load memory cells with CMOS peripheral logic, to give you the speed you need at the power dissipation you want.

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Fast solutions for your high speed memory applications are available today from Mitsubishi. For technical data, call or write Mitsubishi Electronics America, Inc., Semiconductor Division, 1050 East Arques Avenue, Sunnyvale, CA 94086. (408) 730-5900, Ext. 2314.

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CIRCLE NO 94

GRAPHICS BOARD

The GESVIG-4 is a single-Eurocard graphics-display controller for the G64 or G96 Bus. The board, which is based on the HD63484 color-graphics controller, is capable of displaying a 640×480-pixel image from its 380k-byte frame buffer. It provides 8 bits/pixel, allowing you to display as many as 256 colors from a palette of 256,000.

The board executes 38 graphics commands, including 23 drawing commands, a conditional drawing function for generating patterns, color mixing, and software-controlled windowing functions. It also features line-by-line scrolling and step-by-step panning of the image.

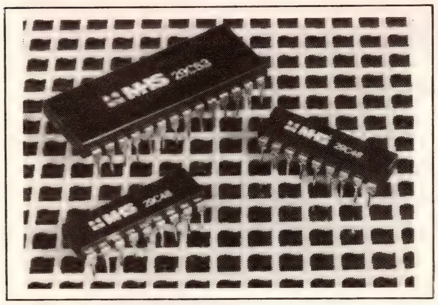
Software support for the GESVIG-4 board is provided by the GPS-III graphics software package, which provides high-level graphics functions that are callable from Pascal, C, Basic, Fortran, or assembly-language programs. GESVIG-4, $1200 (100); GPS-III, $250.

Gespac sa, 3 Chemin des Aulx, 1228 Geneva/Plan-les-Ouates, Switzerland. Phone (022) 713400. TLX 429989.

Circle No 682

Gespac Inc, 100 W Hoover Ave, Mesa, AZ 85202. Phone (602) 962-5559. Hall 18, Stand 18-D-10

Circle No 683



TELECOMM ICs

The 29C48 and 29C53 telecommunications ICs provide line-card and terminal interfaces for ISDN equipment. The 29C48 is a monolithic codec/filter that interfaces an analog line to the digital network by performing PCM coding, decoding, and voice-path filtering. The device also offers user-selectable A-law or μ-law correction, activation of a secondary analog input channel, and programming of transmit and receive gain. The 29C48 is housed in an 18-pin ceramic package and costs around $14 (100).

The 29C53 digital-loop controller operates at either end of the normalized S interface (CCITT recommendation I.430). It performs physical frame formatting between the S-point, 4-wire loop and the SLD Bus. In addition, the device performs D-channel processing (HDLC framing) through its μP interface or SLD interface ports. In a multipoint system, you can connect as many as eight devices to the S line on the terminal side of the ISDN interface. The 29C53 interfaces directly to the 29C48 PCM codec/filter via the SLD Bus. Housed in a 28-pin package, the part costs around $21 (100).

Matra-Harris Semiconducteurs, La Chantrerie, Route de Gachet, 44075 Nantes Cedex, France. Phone (40) 303030. TLX 711930.

Circle No 670

Matra Design Semiconductor, 2840-100 San Tomas Expressway, Santa Clara, CA 95051. Phone (408) 986-9000. Hall 19, Stand 19-A-05

Circle No 671

SMD CAPACITORS

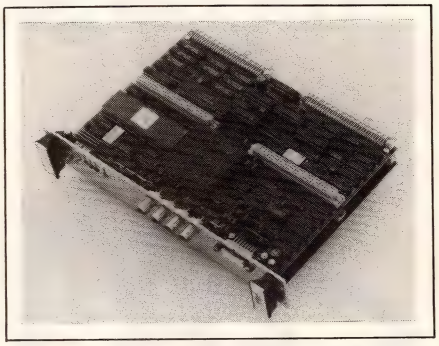
Metallized-film SMD capacitors in the MKS-01-SMD range use a polyethylene terephthalate dielectric and are available with capacitance values from 0.01 to 0.1 μF. The capacitors have a voltage rating of 50V dc, and they're available with ±20 or ±10% tolerance on their nominal capacitance values.

Each capacitor fits into a flame-retardant, 5.7-mm plastic case, which has the same mounting dimensions as that of a ceramic chip capacitor. The 0.01 and 0.047 μF capacitors are 2.5 mm high and 6 mm wide. The corresponding dimensions for capacitors with higher values are 3 and 7 mm. The devices withstand a solder-bath temperature of 260°C for 4 sec.

At 20°C, the capacitors spec insulation resistance greater than 3.75 GΩ and dissipation factors (tan δ) of 8×10^{-3}, 20×10^{-3}, and 30×10^{-3} or less at frequencies of 1, 10, and 100 kHz, respectively. The capacitors operate over −55 to +100°C and are suitable for application class FME in accordance with DIN-40040. Around $0.17 (1000) for a 0.047 μF, 20%-tolerance capacitor.

Wilhelm Westermann-Wima, Augusta-Anlage 56, 6800 Mannheim 1, West Germany. Phone (0621) 408012. TLX 462237. Hall 21, Stand 21-C-10

Circle No 681



VME GRAPHICS CARDS

Based on the 63484 color-graphics controller, the SYS68K/AGC-1 VME Bus graphics-controller subsystem provides 1600×1280-pixel, 50-Hz interlaced or 1024×800-pixel, 50- or 60-Hz noninterlaced display formats. The 4 bits/pixel and onboard color look-up table allow you to display as many as 16 colors from a palette of 16 million. To display as many as 256 colors from the 16-million-color palette, you can reduce the display resolution to 800×600 pixels (50 Hz, noninterlaced) or 720×560 pixels (50 or 60 Hz, noninterlaced) and operate with 8 bits/pixel.

The subsystem comprises two double-Eurocard-size VME Bus boards mounted on a single front panel. It has 2M bytes of hardware-refreshed dynamic RAM, which is ported to both to the VME Bus and the graphics-controller chip. For

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LEMO USA INC

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CIRCLE NO 95

Mounting power semiconductors...

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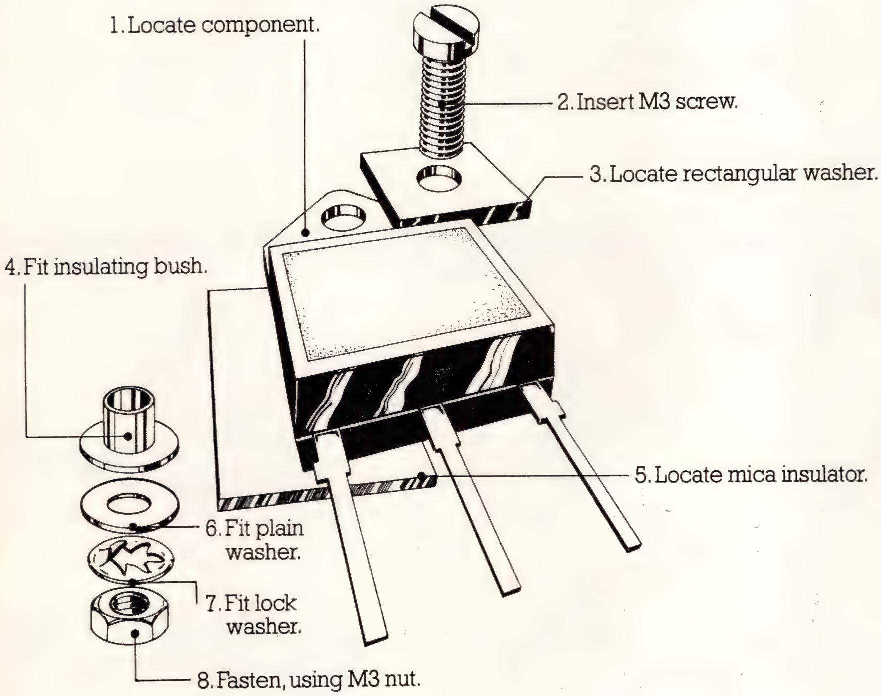
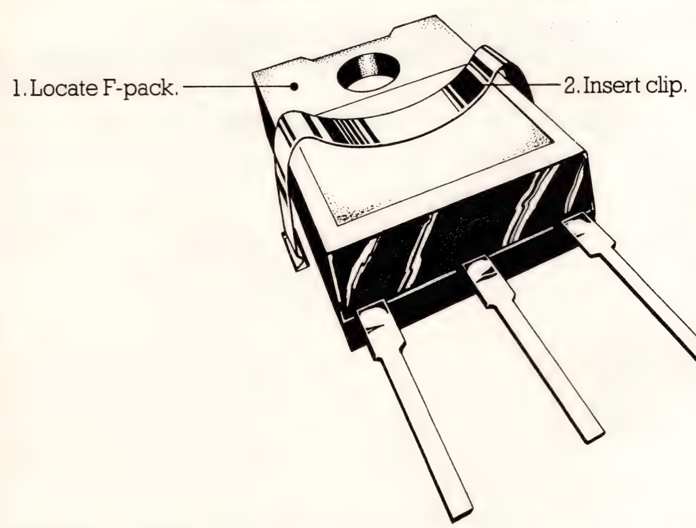


...and the F-Pack way



Just compare the speed and simplicity of mounting F-Pack power semiconductors with conventional methods...

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Philips F-Packs have an integral epoxy insulating layer, which eliminates the need for a mica insulator and all the fiddly insulating bushes, screws, nuts and washers that go with it. The packages can be secured with a single clip or a much-simplified screw assembly, the latter requiring the minimum of heatsink machining.

What's more, the thermal and electrical characteristics of the two F-packs, SOT-186 and SOT-199, are as good as the TO220 and SOT-93 which they can replace.

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If you'd like to know more about the ways in which F-Pack power semiconductors could help you speed production and improve your product's safety and reliability, just contact your local Philips National Organisation.
Or contact Philips Electronic Components and Material Division,
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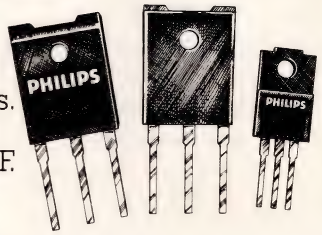

The name is Philips.
The product is power semiconductors.

PHILIPS Electronic components and materials

PHILIPS

CIRCLE NO 66

split-screen operation, you can define three different screen areas with software-programmable positions. Pixel-by-pixel scrolling is provided for both vertical and horizontal soft scrolling.

A GKS (Graphics Kernel Standard) software interface for the subsystem is available for running under Unix or PDOS; it allows you to interface the SYS68K/AGC-1 to Fortran 77 or C programs. DM 12,954.

Force Computers GmbH, Daimlerstrasse 9, 8012 Ottobrunn/Munich, West Germany. Phone (089) 600910. TLX 524190.

Circle No 672

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410. Hall 22, Stand 22-E-12

Circle No 673

POWER MOSFETs

ZVN32 Series n-channel enhancement-mode power MOSFETs are capable of carrying a drain current as high as 18A. The three types currently available, the ZVN3206L, ZVN3210L, and ZVN3220L, have drain-source breakdown voltages of 60, 100, and 200V. Their on-resistance specs are 0.12, 0.18, and 0.5Ω respectively. The ZVN3206L and ZVN3210L are BS/CECC approved. The MOSFETs are housed in TO-220 packages, which allow them to dissipate as much as 75W. Around £1 (1000).

Ferranti Electronics Ltd, Fields New Road, Chadderton, Oldham, Lancashire OL9 8NP, UK. Phone 061-624 0515. TLX 668038.

Circle No 688

Ferranti Electric Inc, 87 Modular Ave, Commack, NY 11725. Phone (516) 543-0200. Hall 24, Stand 24-A-6

Circle No 689

ECL GATE ARRAYS

ELA6000 Series ECL gate arrays let you design ASICs having gate propagation delays as short as 180 psec and system clock frequencies higher than 1 GHz. The flip-flops can toggle at more than 2 GHz. The manufacturer currently offers arrays that let you produce 2900 equivalent 2-input gates. Arrays having 1000 and 4500 equivalent gates are scheduled for the first quarter of 1987.

For each gate, you can define one of three speed/power ratios. On a −4.5V supply, the power dissipation for 180-psec gate delays is 7.2 mW/gate. Selecting the 280- or 560-psec gate-delay options decreases power dissipation to 3.6 mW/gate and 1.8 mW/gate respectively. As long as you don't exceed the package's power-dissipation limit, you're free to mix the various speed/power ratios on the same array. The array has two metal layers available for routing; the manufacturer recommends

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CIRCLE NO 15

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The UTD family from UTMC sets itself apart from the crowd. It's attracting attention with high speed and density wrapped into a rugged gate array designed specifically for military and aerospace applications.

By specifying our UTD family, your system will stand out with performance advantages made possible by 1.25μ effective channel length and sub-nanosecond gate delays. And you have more than 11,000 useable gates with our patented continuous-column architecture making it one of the densest 1.5μ military arrays available.

The UTD series uses proven double-level-metal CMOS technology and is screened to selected tests in MIL-STD-883C.

This family is available for design now using UTMC's proprietary VAX™-based HIGHLAND℠ CAD system. And, we offer our design tools free of charge when you design with our gate arrays.

At UTMC, we recognize your individual needs and support them with fully-equipped design/service centers and applications experts in Boston, Los Angeles, and Colorado Springs.

Take a closer look at our 1.5μ CMOS military gate array. We're not just another pretty face.

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Microelectronics Center
1575 Garden of the Gods Road
Colorado Springs, Colorado 80907
1-800-MIL-UTMC
Boston Design Center
(617) 890-8862
Los Angeles Design Center
(213) 338-0008

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

CIRCLE NO 97

interactive placement for optimum system performance.

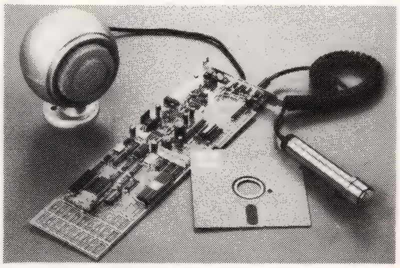
To design with the ELA6000 arrays, you can use the company's VAX-based Classic software. A basic package for net-list or schematic entry, simulation, test verification, and test-tape generation costs around £25,000. The MLE software package, which costs around £100,000, provides the facilities of the Classic package as well as placement and routing, and it produces a data file suitable for PG-tape generation. Engineering costs for 10 prototypes come to around £20,000; production pieces cost around £100 (5000).

Plessey Semiconductors Ltd, Cheney Manor, Swindon, UK. Phone (0793) 36251. TLX 449637.

Circle No 668

Plessey Semiconductors, 3 Whatney, Irvine, CA 92718. Phone (714) 951-5212. Hall 25, Stand 25-B-8

Circle No 669

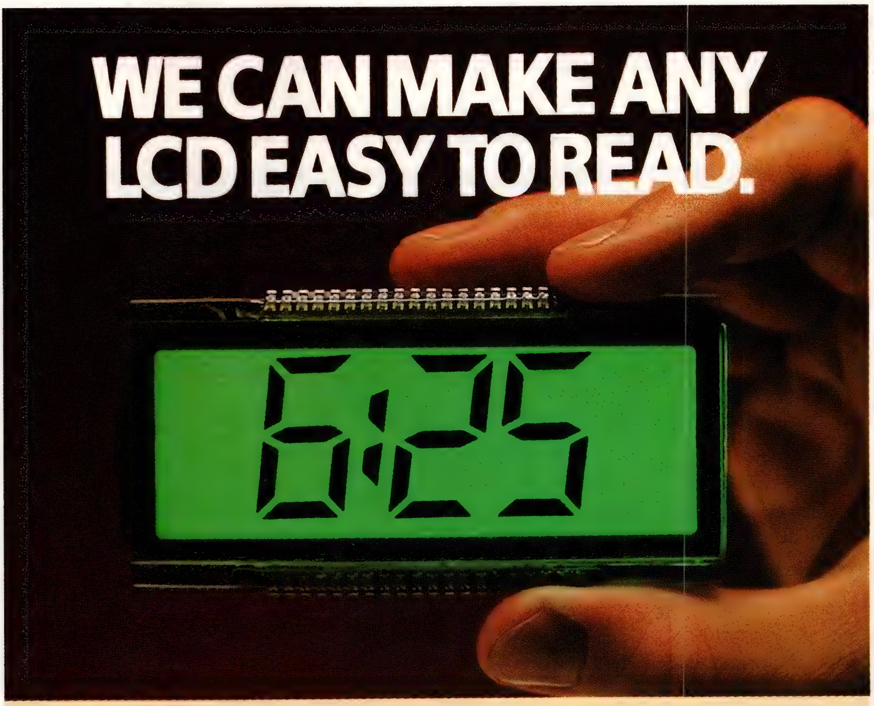


PC SPEECH CARDS

The Audiocard-300, -310, and -600 plug-in cards allow you to add speech-recording/playback and speech-recognition facilities to the IBM PC, PC/XT, PC/AT, or a compatible computer. The Audiocard-300 and -310 use CVSD (continuously variable slope delta-modulation) encoding/decoding to provide record/playback facilities. Digitized speech information, which is transferred into the PC's memory, requires around 3k bytes for each second of recorded sound.

In addition to record/playback facilities, the Audiocard-600 provides a speech-recognition function. The card uses PCM encoding/decoding along with data compression/decompression. You can trade speech quality for memory requirements by selecting the encoder's data rate to 24k, 32k, or 64k bps. You can program the board to recognize as many as 128 words. It stores recognizable words in four 16k-byte blocks of onboard CMOS memory, each of which can hold the results of one training session. During speech recognition, the board achieves an average response time of 0.5 sec and a recognition accuracy of better than 98%.

Menu-driven software for the IBM PC comes with the boards, as do drivers for compiled Basic or Pascal programs. The Audiocard-



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Luminescent Systems Inc.
Setting the Standard
Tel. (603) 448-3444 TWX 710-366-0607
Etna Rd., Lebanon, NH 03766

CIRCLE NO 54

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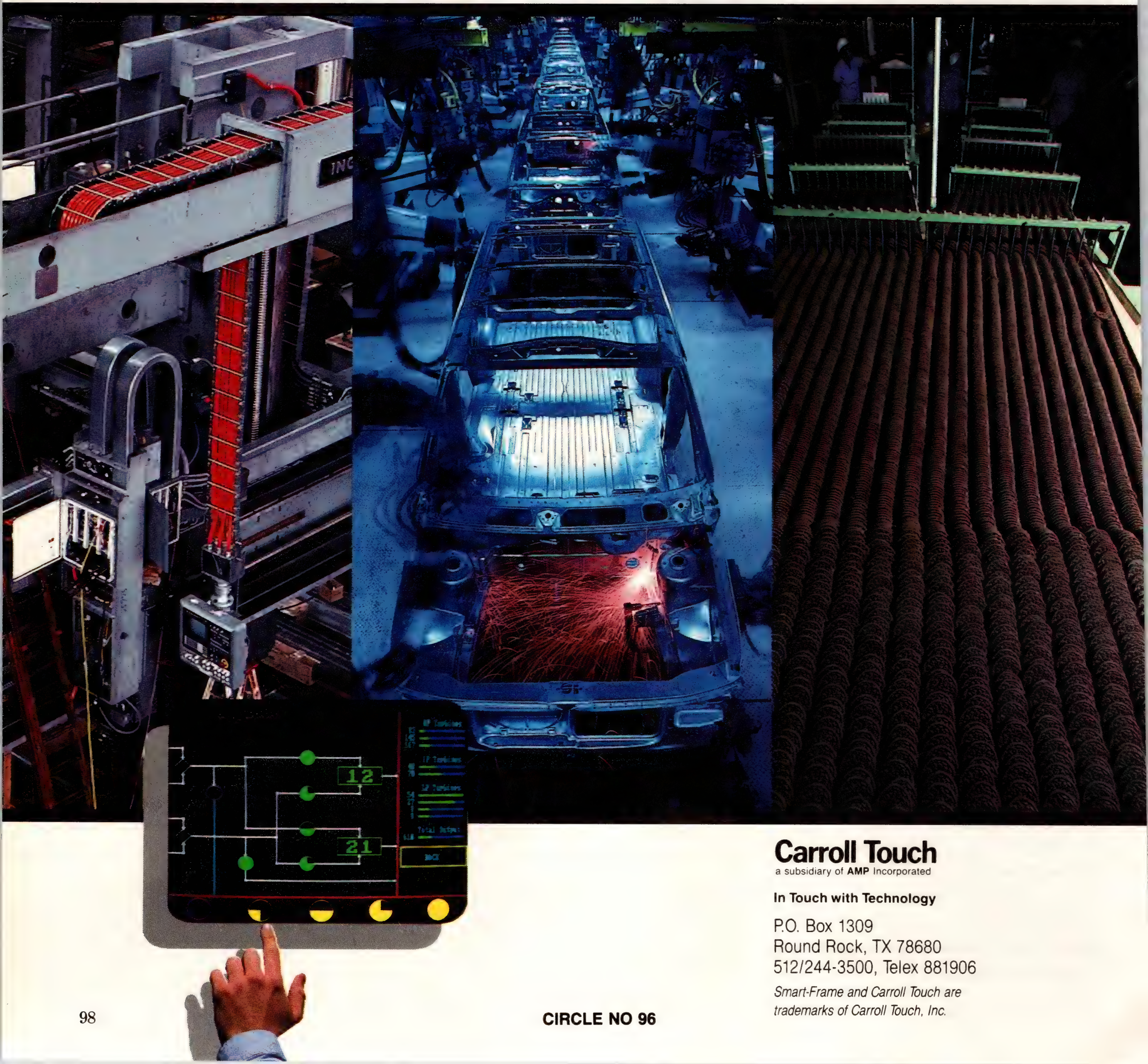

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CIRCLE NO 96

310 and -600 include a battery-backed real-time clock and an RS-232C-compatible port. Audiocard-300, DM 860; -310, DM 980; -600, DM 2000.

Speech Design, Landsberger Strasse 33, 8034 Germering, West Germany. Phone (089) 849310. TTx 898931. Hall 22, Stand 22-B-14

Circle No 674

POWER ICs

Allowing you to drive dc brushless motors and voice-coil actuators with two ICs and a minimum of external components, the IP3M05 and IP3M11 smart-power ICs are suitable for motor-speed and head-positioning control in disk-drive assemblies.

The IP3M05 provides control and drive circuitry to run 12V dc brushless motors. The device accepts rotor-position information from Hall-effect sensors, so it can commutate its 3-phase push-pull motor-winding drivers. The IC controls motor speed by comparing the motor's actual speed, which is sensed by the Hall-effect sensors or a separate tachometer, with a reference frequency. The IC maintains the correct speed via linear control of the motor-winding current to a predefined value. The driver's maximum output current is 2.5A. It also features separate 5 and 12V supplies for the logic and drive circuitry, integral flyback diodes on the outputs, and thermal-shutdown circuitry. The IP3M05 is packaged in a 20-pin power SIP and is priced at £4.00 (50,000).

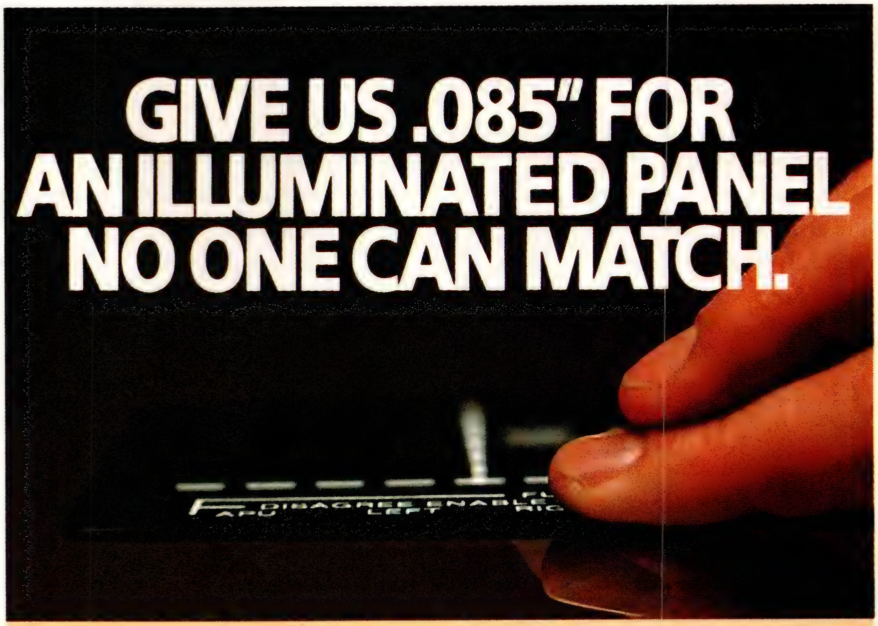
The H-bridge output stage of the IP3M11 power transconductance amplifier is capable of driving as much as 3A into voice-coil-operated disk-head-positioning actuators. The amplifier accepts a single-ended or differential input signal with a maximum swing of ±3V, and you set its transconductance value with two external sense resistors. Two external capacitors set the amplifier's bandwidth. A TTL-compatible input lets you retract the disk head by driving the voice coil with a constant current, and a separate power-supply input lets you retract the head during power-down conditions. The IP3M11 is packaged in a 14-pin power SIP and costs £3.75 (50,000).

Integrated Power Semiconductors Ltd, MacIntosh Rd, Kirkton Campus, Livingston EH54 7BW, UK. Phone (0506) 416416. TLX 727360.

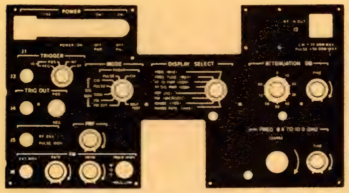
Circle No 675

Integrated Power Semiconductors, 2727 Walsh Ave, Suite 201, Santa Clara, CA 95051. Phone (408) 727-2772. Hall 21, Stand 21-B-15

Circle No 676



At only .085" thick, our new fiberglass electroluminescent panels are designed to replace lightplates and traditional metal plates that may not presently be illuminated. Our thin .085" panels weigh 40% less than a typical .220" plexiglass panel, and with an expansion coefficient equal to aluminum, the panels are ideal for surface-mount applications.


LSI electroluminescent panel

As the pioneer developers of EL lamps, as well as the process of encapsulation, we have combined the uniform, cool surface illumination of EL with the strength of fiberglass to create a new standard for panels.

Durability and long life luminescence

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If you'd like a copy of our brochure, or have questions regarding panel applications, just call, write or TWX the LSI Marketing Department.

Luminescent Systems Inc.
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Etna Rd., Lebanon, NH 03766

CIRCLE NO 93

POWER-SUPPLY ICs

The IP1P00 and IP1P01 ICs form a 2-chip set for use in off-line switch-mode power supplies. The IP1P00 provides drive circuitry for the supply's primary-side MOS switching transistor while the IP1P01 monitors the output on the secondary side and provides the necessary PWM feedback for output regulation. The feedback between the IP1P01 and the IP1P00 is transformer-coupled via single turns on a low-cost toroid, which maintains isolation between the primary and secondary sides of the supply. The IP1P00 features a maximum duty-cycle limit on its PWM output, cycle-by-cycle current limiting, undervoltage lockout with hysteresis, and soft-start and external synchronization capabilities. The IP1P01 secondary-side controller has a 1.25V, 1% internal reference and dc-output current-limiting circuitry. The 2-chip set sells for around £2.40 (50,000).

Integrated Power Semiconductors Ltd, MacIntosh Rd, Kirkton Campus, Livingston EH54 7BW, UK. Phone (0506) 416416. TLX 727360.

Circle No 686

Intergrated Power Semiconductors, 2727 Walsh Ave, Suite 201, Santa Clara, CA 95051. Phone (408) 727-2772. Hall 21, Stand 21-B-15

Circle No 687

DATA-ACQUISITION IC

The ZN437 is an 8-bit, 8-channel data-acquisition system in a single 28-pin IC. It consists of an 8-channel input multiplexer, an 8-bit successive-approximation A/D converter, and an 8×8-bit data RAM. The device has a 3-state TTL/CMOS-compatible bidirectional μP interface, which allows you to program the system and to interrogate the results of channel conversions stored in the RAM. You can program the device to execute a single conversion on a named input channel, to convert continuously on one channel, to perform one conversion on all eight channels, or to convert continuously on all eight channels.

A programmable clock divider allows you to scale clock frequencies as high as 4 MHz to a clock rate suitable for the 20-μsec A/D converter. The ZN437 is available in two versions having linearity errors of ±½ or ±1 LSB. Corresponding differential linearity error for the two versions is ±¾ and ±1 LSB, respectively. The multiplexer's analog inputs accept inputs between −0.5 and +3.5V and draw a typical input bias current of 10 nA. The device requires an external voltage reference of between 1.5 and 3V.

Now, implement GPIB systems faster. If you're putting together GPIB systems based on PCs, here's good news. Now you can interconnect any of the over 4,000 IEEE 488-compatible devices faster than ever before. With hardware controllers that transfer data at 450 Kbytes/second, and complete development support from Ziatech.

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You also have access to applications support that's second to none. With complete, up-to-date hardware/software documentation.

ZIATECH CONTROL: FROM

The ZN437 operates from a positive 5V supply and a negative supply from −2 to −30V. It draws 45 mA typ from the 5V supply. It is packaged in a 28-pin plastic or ceramic DIP that's specified for operation over the commercial or military temperature ranges. £8.20 (100) for a commercial-grade, ±1-LSB-linearity version.

Ferranti Electronics Ltd, Fields New Road, Chadderton, Oldham, Lancashire OL9 8NP, UK. Phone 061-624 0515. TLX 668038.

Circle No 679

Ferranti Electric Inc, 87 Modular Ave, Commack, NY 11725. Phone (516) 543-0200. Hall 24, Stand 24-A-6

Circle No 680

CODECS

The FX609 and FX709 are CVSD (continuously variable slope delta-modulation) codecs that allow you to implement a full-duplex, digitally encoded voice channel or to store and retrieve audio information from digital memory.

The FX609 codec has separate coder and decoder sections that digitize and reconstruct an analog voice channel before and after the transmission of a digitally encoded signal. The chip has lowpass filters before the coder and after the decoder. The codec has an on-chip oscillator for a 1.024-MHz crystal; it can also accept an external clock source. You can pin-program the codec to operate with a 16k-, 32k-, or 64k-bit/sec sampling rate and to select a 3- or 4-bit companding algorithm. The IC's control inputs allow you to force the coder output or decoder input to an 0101 idle condition, and force the coder output to a high-impedance state.

The coder section of the FX709 voice-store/retrieval codec converts an analog audio input into 8-bit CVSD-encoded words for storage in byte-wide memory. Its decoder section reconverts the stored bytes of information into an audio output.

A μP interface allows you to control the codec via internal control and status registers. Both the FX609 and FX709 are 5V CMOS devices and are priced at around £6 and £10 (1000), respectively.

Consumer Microcircuits Ltd, 1 Wheaton Rd, Witham, Essex CM8 3TD, UK. Phone (0376) 513833. TLX 99382.

Circle No 677

Mx-Com Inc, 8060-F N Point Blvd, Winston-Salem, NC 27106. Phone (919) 744-5050. Hall 18, Stand 18-C-8

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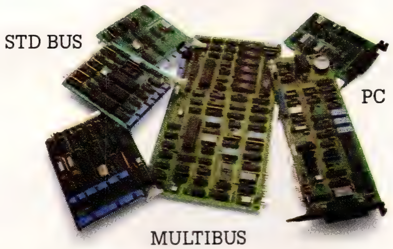

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Tomorrow's Challenge: developing innovative tools for characterizing the physical and thermal properties of newly engineered materials, and protecting those tools in instrumentation systems around the world.

Illustration of Dupont 9900 Thermal Analysis systems. Dupont Company, Instrument Systems Division, Wilmington, Delaware

CIRCLE NO 16

Your VME system just got faster.

Eleven new VMEbus modules from Dual can make your 32-bit designs take off. Today.

Dual's full line of VMEbus modules is setting new performance and packaging standards in the 32-bit world. Especially among applications that demand high system throughput, fast I/O processing and heavy disk usage.

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These modules are all fully ruggedized, housed in a standard VME backplane, and run under a system controller featuring fast 96ns arbitration. For software support, our implementation of UNIX System V, Release 2.0, Version 2 is available.

So why waste time developing your own 32-bit VMEbus solutions when ours are ready to go? For full details, contact: Dual Systems Corporation, 2530 San Pablo Ave., Berkeley, CA 94702. (415) 549-3854. Telex 230199 SWIFT.

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CIRCLE NO 99

Wescon/86 will highlight CAE applications and high-speed analog and digital ICs

Margery S Conner,
Regional Editor

Engineers who attend Wescon/86 will have the opportunity to view the latest electronic-product innovations and get tips on their applications and design criteria. Despite the recent tendency of electronic trade shows to focus on one narrow aspect of the electronics market, Wescon remains one of the few conferences that still covers the broad spectrum of electronics. This year's conference will take place November 18 through 20 in Anaheim, CA (see **box**, "Wescon/86 registration details" for more information).

The conference program will strongly emphasize two areas: the design of high-speed analog and digital ICs, and the application of CAE/CAD equipment, particularly in PLD design. However, virtually all areas of electronics will be represented. Session topics will include such subjects as networks, 32-bit microprocessors, robotics, and graphics, for example.

Enhancing system performance

WESCON/86 TECHNICAL SESSIONS, ANAHEIM HILTON HOTEL, ANAHEIM, CA

		CALIFORNIA BALLROOM		PACIFIC BALLROOM		
		C	D	B	C	D
TUESDAY, NOVEMBER 18	9:00 TO 11:00 AM	1 IEEE-488 PROGRAMMING SOLUTIONS	2 LOCAL-AREA NETWORK MEDIA: OFFICE-FACTORY STANDARDIZATION, CHARACTERISTICS, AND MODELING	3 VLSI GRAPHIC DEVICES	4 NOVEL RAM ARCHITECTURES AND RAM-SUPPORT CIRCUITS CHALLENGE NEW APPLICATION DOMAINS	
	12:30 TO 2:30 PM	5 USING ADA IN REAL-TIME APPLICATIONS	6 ISDN PROGRESS REPORT: PART I—STANDARDS AND PRODUCT IMPLEMENTATION	7 ENHANCE YOUR SYSTEM PERFORMANCE WITH GALLIUM-ARSENIDE DIGITAL DEVICES	8 INTELLIGENT/APPLICATION -SPECIFIC MEMORY	
	3:30 TO 5:30 PM	9 USING UNIX IN REAL TIME	10 ISDN PROGRESS REPORT: PART II—USER EVALUATION AND FIELD TRIAL ACTIVITY	11 ECL BUILDS HIGH-PERFORMANCE SYSTEMS	12 APPLICATION-SPECIFIC MEMORIES: NEW OPPORTUNITIES IN ASICs	
WEDNESDAY, NOVEMBER 19	9:00 TO 11:00 AM	13 SURFACE-MOUNT TECHNOLOGY	14 BUILDING NUMBER CRUNCHERS WITH LSI DATA-PATH ELEMENTS	15 UTILIZING ADVANCES IN HIGH-SPEED AMPLIFIERS	16 INNOVATIVE APPLICATIONS WITH ALTERABLE MCUs	17 CONTINUING ENGINEERING EDUCATION: IT REALLY MAKES A DIFFERENCE
	2:30 PM 12:30 TO	18 SOFTWARE QUALITY ASSURANCE IN SOFTWARE DEVELOPMENT	19 NEW ALTERNATIVES IN USER-PROGRAMMABLE LOGIC DEVICES AND SUPPORT	20 ICs FOR MOTION CONTROL ARE MAKING A MOVE	21 ONBOARD SERIAL DATA TRANSMISSION TECHNIQUES IN MCU SYSTEMS	22 ADVANCED CMOS LOGIC IN HIGH-PERFORMANCE SYSTEMS
	3:30 TO 5:30 PM	23 PROTECTING SOFTWARE AND COMMUNICATIONS	24 PROGRAMMABLE LOGIC DEVICES	25 ADVANCES IN ROBOTIC TECHNOLOGY	26 RECENT DISK-CONTROLLER-IC TECHNOLOGY ADVANCES	27 THE CMOS REVOLUTION EXTENDS BIT-SLICE MICROPROCESSORS
THURSDAY, NOVEMBER 20	9:00 TO 11:00 AM	28 HOW OFFSHORE OPPORTUNITIES CAN IMPROVE YOUR COMPETITIVE EDGE	29 TAKING THE UGLY OUT OF CAD/CAE	30 SERIAL PROTOCOLS FOR DISTRIBUTED CONTROL	31 PROGRAMMABLE DITIAL SIGNAL PROCESSORS—A NEW GENERATION	
	12:30 TO 2:30 PM	32 MARKETING HIGH-TECHNOLOGY PRODUCTS	33 PERSONAL COMPUTER—COMPUTER-AIDED DESIGN FOR PC-BOARD DESIGN	34 SWITCHING AND MULTIPLEXING OF VIDEO SIGNALS	35 FLOATING-POINT COPROCESSORS FOR 32-BIT MICROPROCESSORS	
	3:30 TO 5:30 PM		36 THE ENGINEER'S PC USED AS AN ANALOG CAD/CAE/CAT WORKSTATION	37 COMMON PITFALLS OF FCC REGULATIONS AND HOW TO AVOID THEM	38 TRENDS IN 32-BIT MICROPROCESSOR DIRECTIONS	

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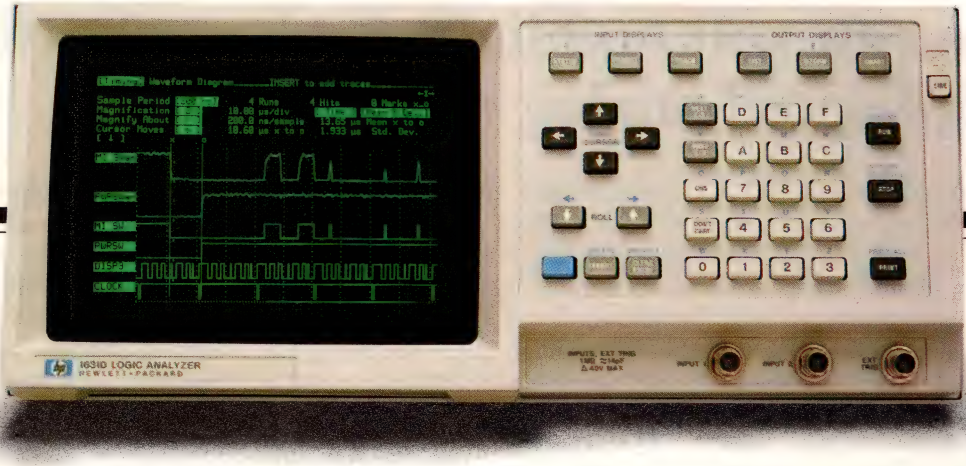

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CIRCLE NO 137

with gallium-arsenide ICs will be the subject of **session 7,** which will be chaired by Fred Cherrick of Gigabit Logic and will include papers from RCA, Triquint, Vitesse Electronics, and Ford Microelectronics. Speakers will consider the future of ECL in **session 11,** entitled "ECL builds high-performance systems." In one of this session's papers, William Blood of Motorola will consider internal memory, which he believes will soon be commonly implemented in ECL arrays. Speakers in **session 22,** "Advanced CMOS logic in high-performance systems," will explore future speed improvements for CMOS. The specific application of CMOS technology in bit-slice computers will be covered in **session 27.**

CAE/CAD tools

Three conference sessions will specifically address CAE/CAD. **Session 29,** for instance, is entitled "Taking the ugly out of CAE/CAD." It will feature papers from Data I/O-FutureNet, HHB Softron, Tektronix, Sperry, and LSI Logic. The reports will examine the impact of CAE/CAD on design and predict future improvements in the area. In **session 33,** speakers from T&W Systems, Orion Instruments, Rio Hondo College, and Calay Systems will discuss personal-computer-based CAD for pc-board design. **Session 36** will also focus on the personal-computer-based workstation, but from an analog-design perspective.

"New alternatives in user-programmable logic devices and support" is the title of **session 19.** In this session, Mike McClure of Data I/O-Futurenet will hold that because PLDs use several thousand gates, and logic arrays easily use more than 30,000, a CAE/CAD software package must be able to work with functional design descriptions. Such descriptions define only what the device must do, not the actual implementation. Functional descriptions are also independent of device type; you can use a PLD to implement a prototype of an initial design and then, after verifying the design, switch to array logic for production parts. Designing with PLDs will be covered in greater detail in **session 24.**

Application-specific RAM

Special-purpose RAM will be the topic of **sessions 4, 8,** and **12.** In **session 12,** "Application-specific memories: New opportunities in ASICs," Pradeep Shah of Texas Instruments will explain that advanced CMOS technologies such as 1-μm line widths will permit the implementation of more than 100,000 transistors and 1M bit of RAM on an application-specific IC (ASIC). In the same session, Bruce Threewit of Advanced Micro Devices will discuss the benefits of dual-array memories in such applications as graphics-display systems, node processing in serial communications networks, and disk caches.

Speakers in **sessions 35** and **38** will continue the discussion of 32-bit-μP technology that took place at last year's conference. Both these sessions will be chaired by Sandra Mazolewski of Intel. **Session 35** will concentrate on floating-point coprocessors for 32-bit μPs; **session 38** will predict the future of these processors.

Engineers interested in digital signal processing will want to attend **session 31,** "Programmable digital signal processors—a new generation," in which representatives of Analog Devices, Signetics, and National Semiconductor will discuss the ADSP-2100, the 5010/5011, and the LM32900, the companies' respective DSP chips. Speakers from NEC and Motorola will also contribute papers to the session. **EDN**

Article Interest Quotient
(Circle One)
High 509 Medium 510 Low 511

Wescon/86 registration details

The Wescon/86 conference and exhibition will take place Tuesday November 18 through Thursday November 20 at the Anaheim Convention Center, Anaheim, CA. General admission is $10 at the door; it covers exhibits, technical sessions, and admission to the film theater for the three days.

Registrants coming from the San Diego and Santa Barbara areas are encouraged to ride Amtrak to the show; free shuttle buses will transport train passengers to the Convention Center. Free shuttles will also run between the Anaheim Convention Center and many of the major local hotels. For more information, contact Electronic Convention Management, 8110 Airport Blvd, Los Angeles, CA 90045. Phone (213) 772-2965.

DIGITAL SCOPE ▶

The HM205 20-MHz digital storage oscilloscope features 1024×256-point resolution, an X-Y mode, and channel inversion. $820.

Hameg Inc, Port Washington, NY
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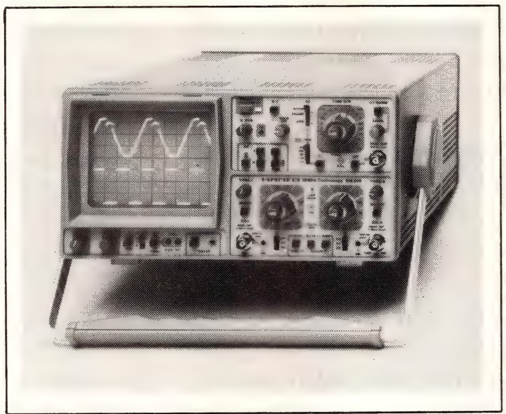

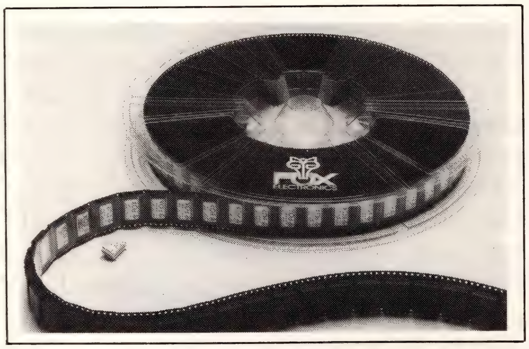

▲ OSCILLATORS

F5C-S7 dual-output oscillators each use two separate crystals to obtain two independent frequencies from one package. $3 to $5.

Fox Electronics, Fort Myers, FL
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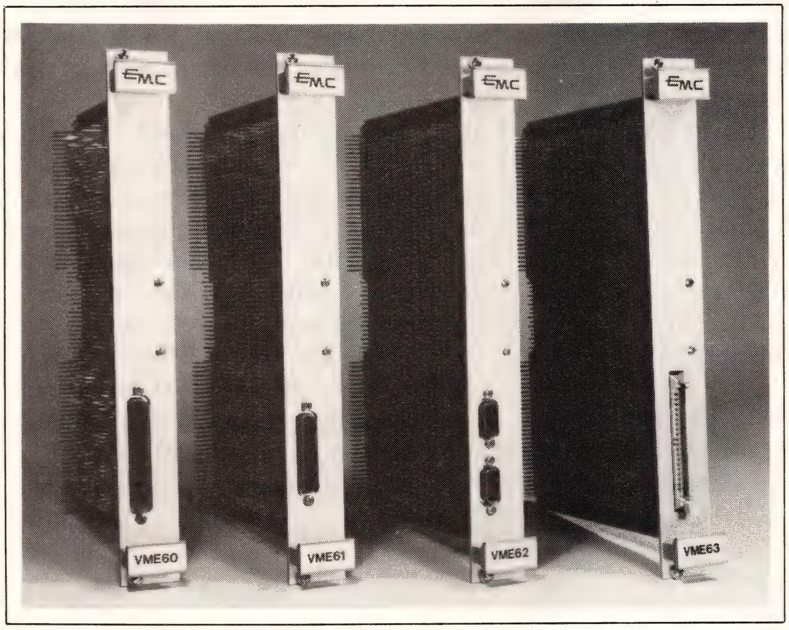

VME BUS PANELS ▲

The VME 60 Series VME Bus panels offer integral decoupling capacitors and front-panel I/O connectors. $315.

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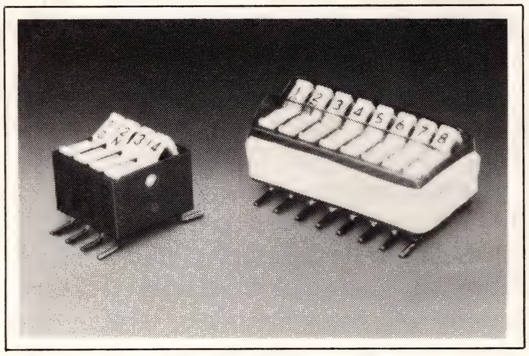

▲ SURFACE-MOUNT SWITCH

The gull-wing configuration of the 2400 Series surface-mount switches permits them to mount on single-layer or multilayer boards. Less than $1 (1000).

EECO Inc, Santa Ana, CA
Booth 2538/2540/2542
Circle No 597

80C31-BASED MODULE ▶

The EDH685C31 μPak Module contains an 80C31 microcontroller, an 8k×8-bit EEPROM, an 8k×8-bit static RAM, and a logic-control unit, all mounted on a 40-pin ceramic substrate. Mil version, $1100.

Electronic Designs Inc, Hopkinton, MA
Booth 1059/1061
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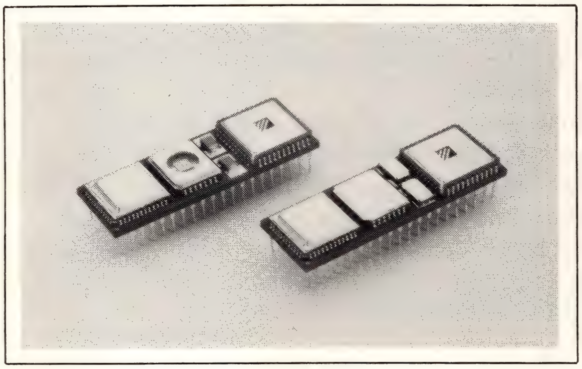

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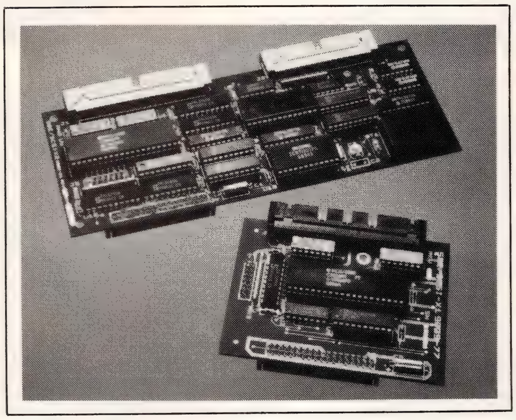
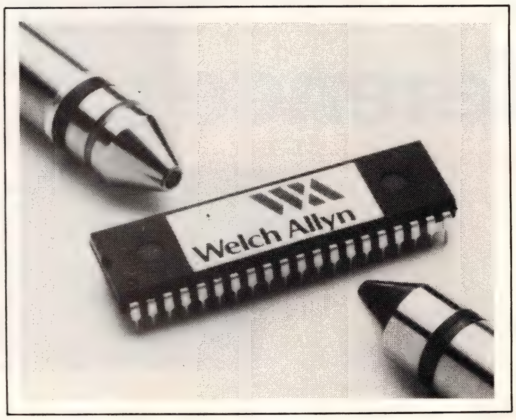


SCSI BOARDS ▲

The SCSI and SCSI-CP Multimodule interface boards support high-speed data transfer to disk and provide general interprocessor communications. The SCSI-CP includes a printer port and a battery-backed clock. SCSI-CP, $320; SCSI, $165 (100).

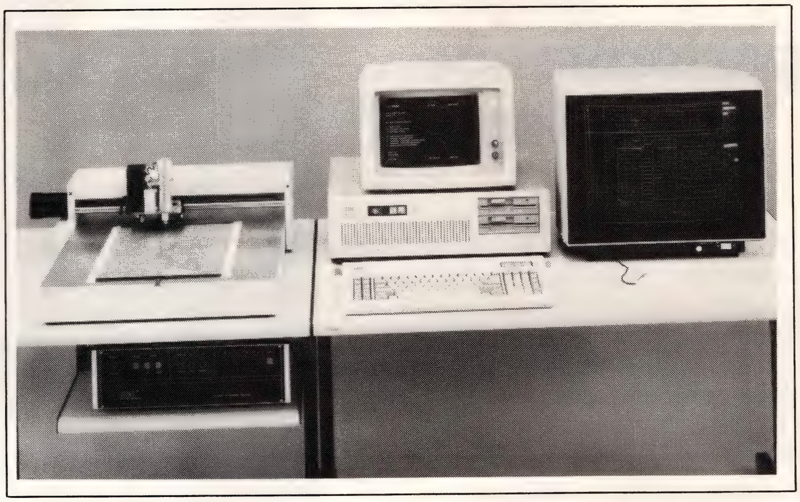
SBE Inc, Concord, CA
Booth 4009/4011
Circle No 590



BAR-CODE DECODER ▲

The LTC-3C, a CMOS single-chip bar-code decoder, can scan high-density codes bidirectionally from 3 to 30 in./sec. $95.

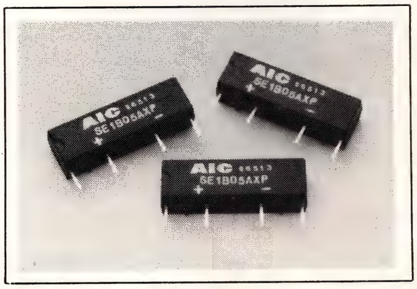
Welch Allyn Inc, Skaneateles Falls, NY
Booth 2139
Circle No 592



▲ CAD/CAM SYSTEM

The ColorCam CAD/CAM system consists of a pc-board design package and an X-Y table that can drill, route, and install feed-through eyelets for prototype boards. $56,000.

LPKF Pacific, Novato, CA
Booth 3278
Circle No 593



REED RELAYS ▲

The Mini-SIP reed relay maintains a 0.2×0.4×0.2-in. pin-grid spacing in a 0.910 × 0.28 × 0.3-in. package. It's available in 5, 12, and 24V versions. $0.94 (1000).

Aleph International Corp, San Fernando, CA
Booth 1274/1276
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WIRE-WRAPPING BOARD ▶

The Super U 366.7×400-mm Schottky-compatible wire-wrapping board holds as many as 56 17×16-pin PGAs. The board comes in versions that support the VME Bus and Multibus II. $2127.

Mupac Corp, Brockton, MA
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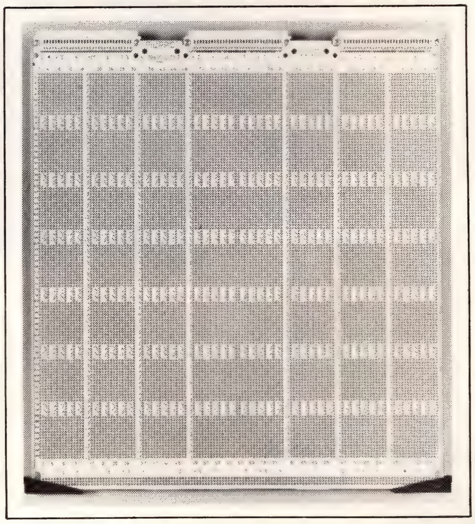

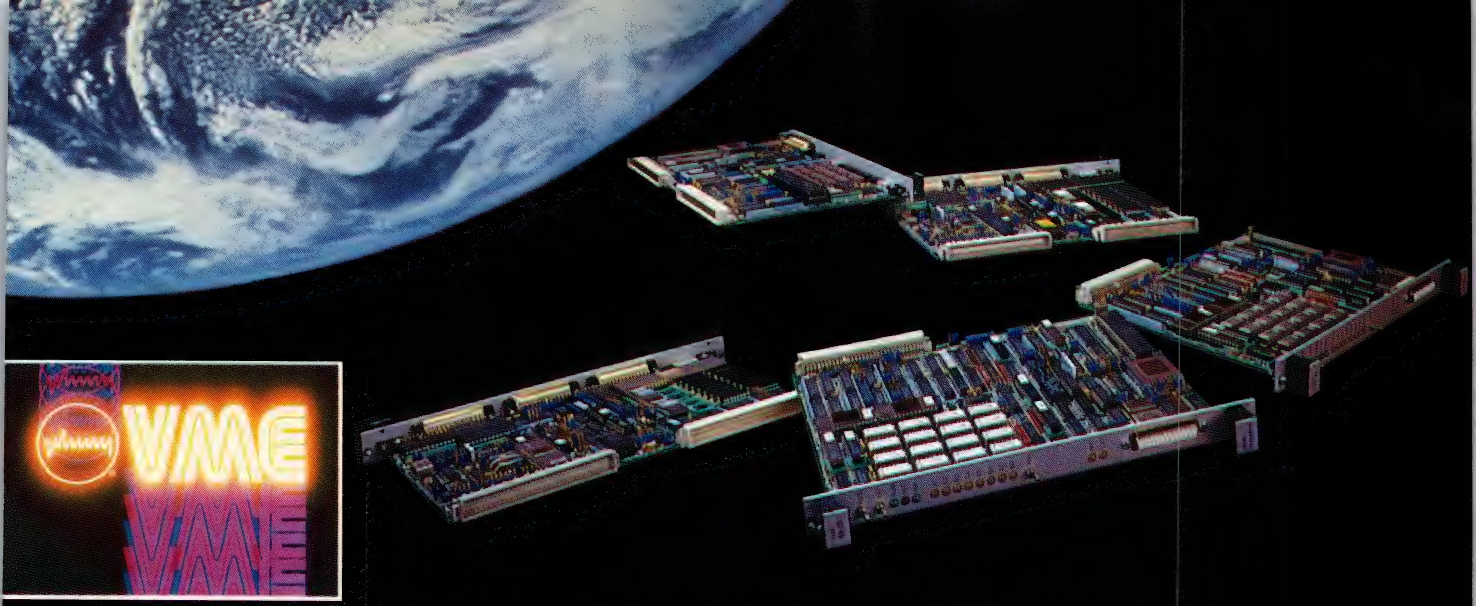

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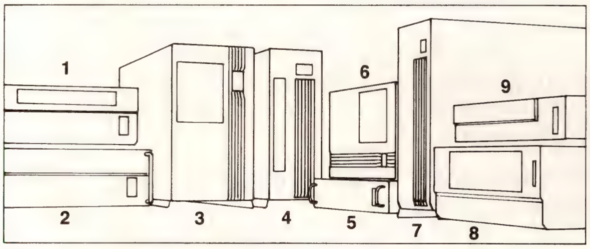

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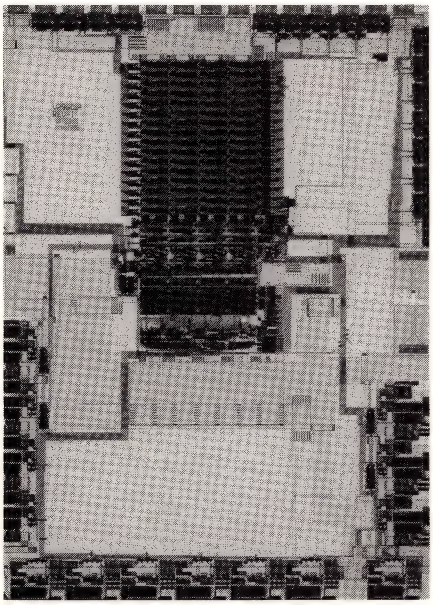
CIRCLE NO 136

GaAs bit-slice µP runs at three times the speed of a silicon version

Operating at three times the speed of bipolar silicon versions, the gallium-arsenide (GaAs) implementation of the Am2900 bit-slice family of microprocessors can execute an instruction in as little as 14 nsec.



The VE29G01 GaAs 4-bit-slice µP *contains approximately 500 logic gates, which include more than 4000 transistors. The processor circuitry is in the center; the 100K ECL-compatible drivers are next to the pins.*

Developed under a technology exchange agreement with Advanced Micro Devices, which originated the 2900 series, the GaAs version is microcode compatible with the silicon version.

The family comprises three chips. The VE29G01 is a 4-bit-slice microprocessor consisting of a 16-word×4-bit, 2-port RAM; a high-speed ALU; and the associated shifting, decoding and multiplexing circuitry. The VE29G02 is a look-ahead carry generator; the VE29G10A is a 12-bit microcontroller that controls the execution sequence of microinstructions stored in microprogram memory. The devices' I/O drivers are compatible with 100K ECL.

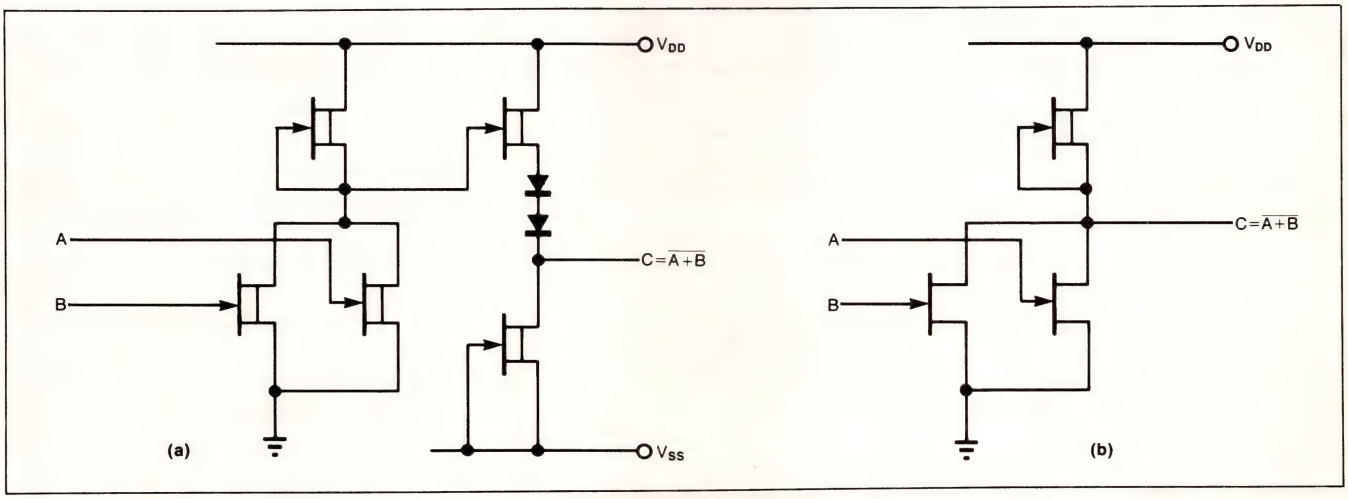
The 4-bit-slice µP performs 4-bit addition in 15 nsec. Its read-modify-write cycle time is 14 nsec, and its maximum clock speed is 72 MHz. The look-ahead carry generator has a carry propagate cycle of 5 nsec. The 12-bit microcontroller supports an address-generation time of 10 nsec and a cycle time of 25 nsec; its maximum clock speed is 100 MHz. The power requirements for all three chips are −2.0 and −4.5V. They operate over 0 to 70°C.

The 4-bit slice and the 12-bit microcontroller each dissipate 1.7W. The look-ahead carry generator requires 430 mW. To reduce power requirements, the devices use enhancement/depletion technology instead of the more common depletion mode. The chips' power consumption is close to that of the silicon 2900 family.

The VE29G01 and VE29G10A come in 52-pin ceramic leadless chip carriers (LCCs); the VE29G02 comes in a 28-pin ceramic LCC. Engineering samples of the VE29G02 ($225) are available within 30 days; samples of the VE29G01 ($435) and VE29G10A ($475) will be available in the first quarter of 1987. Prices for production parts, which will be available later in the year, will be substantially lower, according to the company.—***Margery S Conner***

Vitesse Electronics Corp, 741 Calle Plano, Camarillo, CA 93010. Phone (805) 388-3700.

Circle No 727

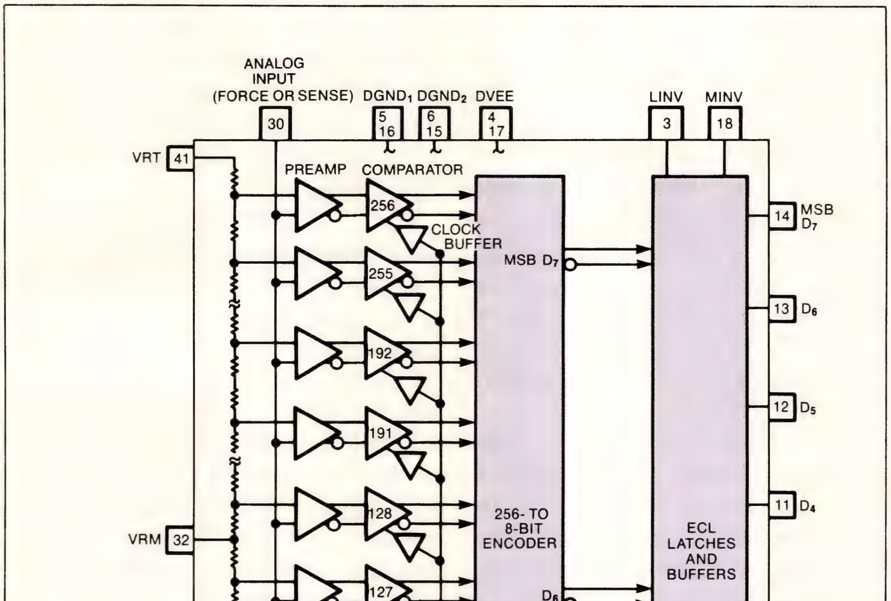


Chips fabricated with enhancement/depletion-mode technology *require only one power supply and typically use a tenth of the power and half the transistors that depletion-mode chips use. A depletion-mode NOR gate* ***(a)*** *employs seven elements, five FETs and two diodes. An enhancement/depletion-mode NOR gate* ***(b)*** *employs only three FETs.*

Monolithic 8-bit flash A/D converter converts at 125-MHz sampling rate

The HADC77100 monolithic 8-bit flash A/D converter is capable of digitizing a 2V analog input signal having components whose frequencies range as high as 70 MHz. The converter accommodates sampling rates as high as 125 MHz. Packaged in a 42-pin ceramic DIP, the IC is pin compatible with Sony's 100-MHz CX20116.

Like the Sony part, the HADC77100 uses one −5.2V supply. As you'd expect, the faster converter dissipates more power than the CX20116—1.7 vs 1.2W. Another difference is the HADC77100's 50Ω ECL-level digital outputs vs the CX20116's 100Ω outputs. To attain its high conversion speed, the HADC77100 requires the use of differential, ECL-level clocks, because the relatively slow edges of TTL-based clock signals could cause hundreds of picoseconds of aperture jitter.



This flash, or parallel, architecture yields a conversion rate of 125 MHz *in Honeywell's HADC77100 8-bit A/D converter. For most applications, you won't need a track/hold amplifier with the converter. ECL-level clocks and digital-output lines contribute to the device's speed.*

You can program the converter's digital outputs to obtain 2's-complement or true- or inverse-binary formats. The HADC77100 contains 255 clocked analog comparators, a tapped reference resistor, encoding logic, and output registers. A single Convert command controls all timing. According to the manufacturer, the converter uses a special comparator design, in which an integral preamplifier minimizes drive requirements and prevents digital transients ("kick-back") from reaching the analog input.

A companion part, Model HADC77200, has user-accessible quarter-scale taps on the resistive reference string, as well as a data-ready terminal that allows you to clock the output data into memory or onto a data bus. Note that you can stack two HADC77100 converters to obtain 9-bit resolution; you will, however, need some additional decoding logic at the two converters' outputs. You can also connect two converters in a "ping-pong" parallel arrangement that uses out-of-phase clocks; this connection effectively doubles the attainable sampling rate. HADC77100, $593.75 (100); HAD77100 evaluation board, $900.—***Bill Travis***

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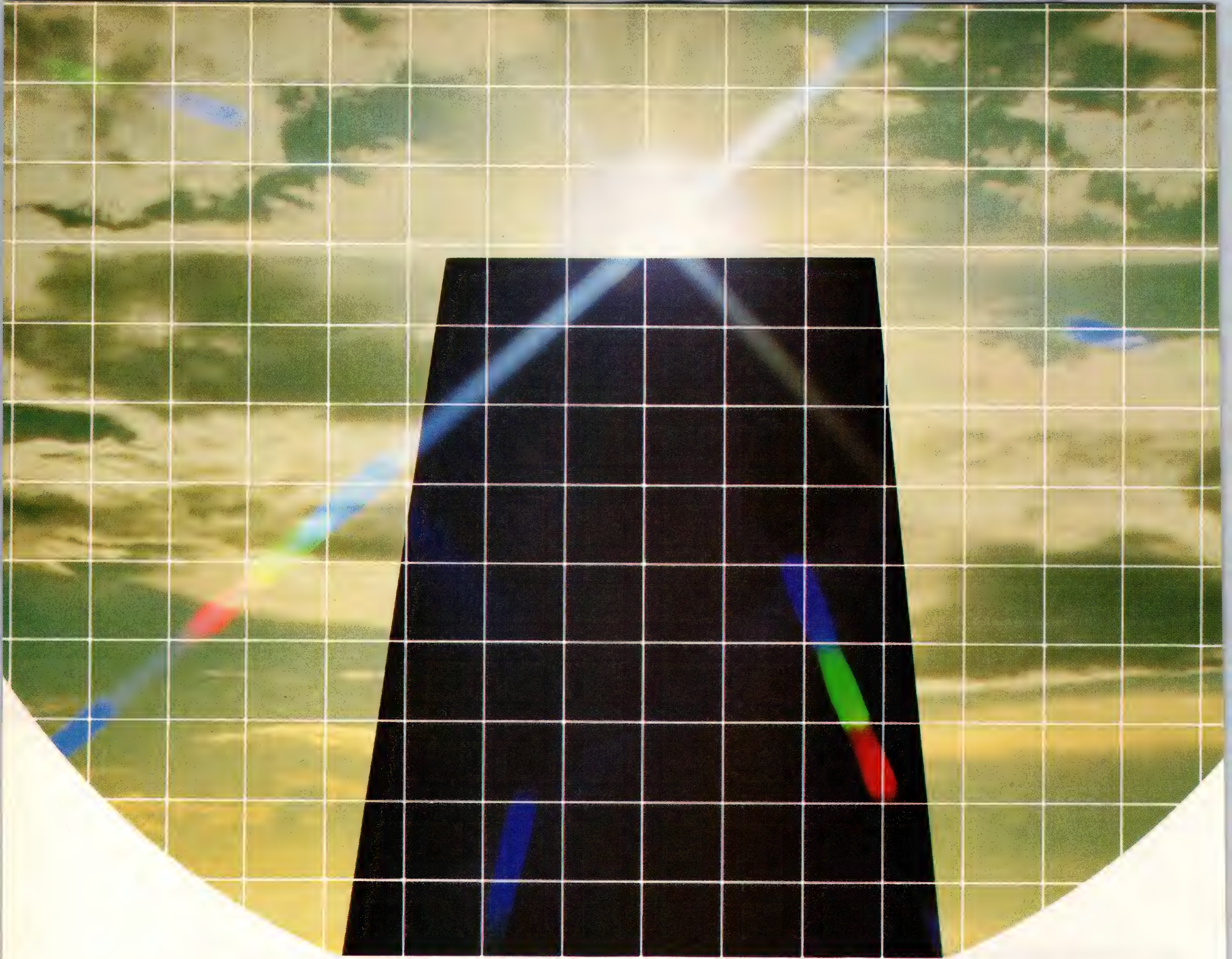

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Software and VLSI hardware offer bit-slice CPU speed

The Accel family of VLSI processors and software tools combines the software-development ease of general-purpose microprocessors with the performance of discrete, microprogrammable bit-slice components. The CPUs provide speeds of 5 MIPS and 10M flops. These speeds, the manufacturer claims, make the CPUs the highest performance high-level-language-driven numeric processors available.

The Accel series comprises three elements. The first element, a complete software-development system, consists of high-level C, Fortran-77, and Pascal compilers, profilers, assemblers, linkers, debuggers, and simulators. The compilers ease your software-development effort by converting the high-level code to object code. A proprietary feature called a "parallelizing instruction scheduler" examines the instruction stream and allocates instructions to the various processing nodes within the CPU.

The second element in the Accel family is a series of CMOS-processed VLSI devices that accommodate the Accel software. These processors use an architecture that's similar to a microprocessor in its high-level-language support, and similar to a microprogrammed bit slice in its wide instruction word. The CPUs' instruction set comprises single-cycle, register-based instructions. Note that the processors execute integer multiple/divide and floating-point add/subtract/multiply/divide operations in silicon hardware, as opposed to using microcoded programs.

Two of the Accel processors will be available in January 1987: the $600 (100) Model 8000-80 and the $1000 Model 8032-80. Both have 32-bit data memories; the 8032-80, however, is a floating-point CPU which has a 64-bit code memory, vs the 8000-80's 32-bit memory. The 8000-80 is an integer-processing unit that's useful for logic simulation, AI processing, or general-purpose computing. The 8032-80 CPU provides 5-MIPS and 10M-flops single-point, floating-point processing for 3-D graphics and DSP applications. The third processor, the 8064-80 ($1500), will be ready in June 1987. It will provide the same speed as the 8032-80, and will perform double-precision, floating-point processing.

The third element in the Accel family is a software-development system. Based on an IBM PC/AT platform, the system has a board set that includes an Accel processor, 4M bytes of program RAM, and code and data caches. The $10,000 system, which will be available in January 1987, includes a resident monitor and debugger to aid in software development.—***Bill Travis***

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Precision quad op-amp IC meets performance of OP-27

Boasting the lowest guaranteed noise of any available quad operational amplifier, Model OP-470 delivers performance that's comparable to that of the manufacturer's industry-standard OP-27. Its 5-nV/$\sqrt{\text{Hz}}$ max noise voltage at 1 kHz, coupled with its 11-mA max supply current, qualifies the device as the industry champion in noise-to-current performance ratio.

The OP-470 also has precision input specs: 0.4-mV max offset and 2-μV/°C max offset drift. And although the amplifier is no speed demon, its 2V/μsec typ slew rate and 6-MHz typ gain-bandwidth product are respectable figures for a precision, low-noise op amp. Other specs that characterize the OP-470 as a high-performance unit are its 1,000,000 min open-loop gain, 110-dB min common-mode rejection ratio, and 1.8-μV/V max power-supply rejection ratio.

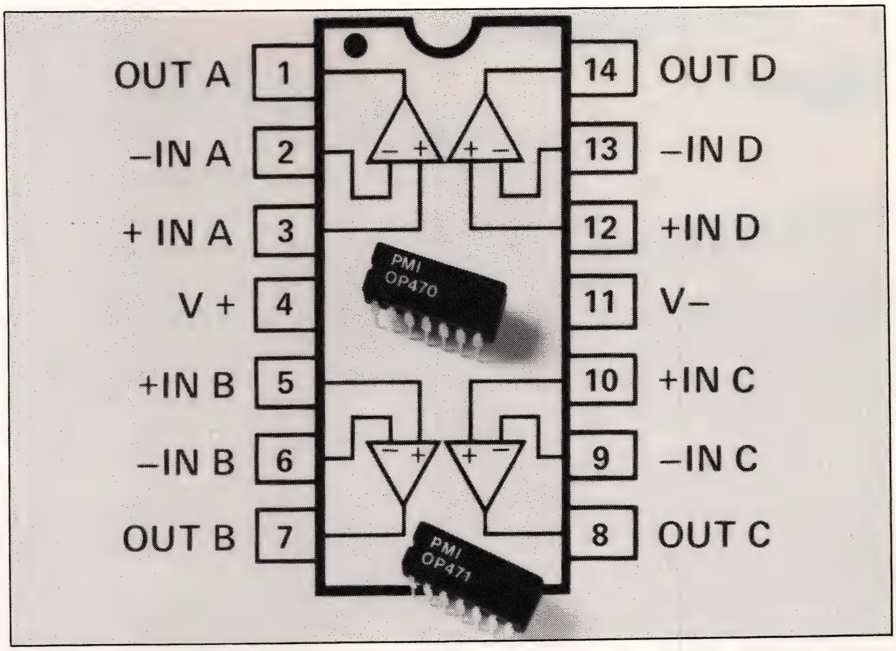
In conformance with the 14-pin industry-standard quad pinout, the OP-470 is compatible with the OP-11, LM148/149, HA4741, HA5104, and RM4156 quad op amps. Its sibling, the OP-471, is a higher speed version of the OP-470. The -471 specs 8V/μsec typ slew rate and 8-MHz typ gain-bandwidth product.

Although the OP-471 (like the OP-470) is unity-gain stable, the higher speed entails some compromises—input offset, drift, and noise are doubled, and the open-loop gain is halved, as compared with the OP-470. Prices for both the OP-470 and -471 range from $6.50 to $17.90 (100), depending on grade.

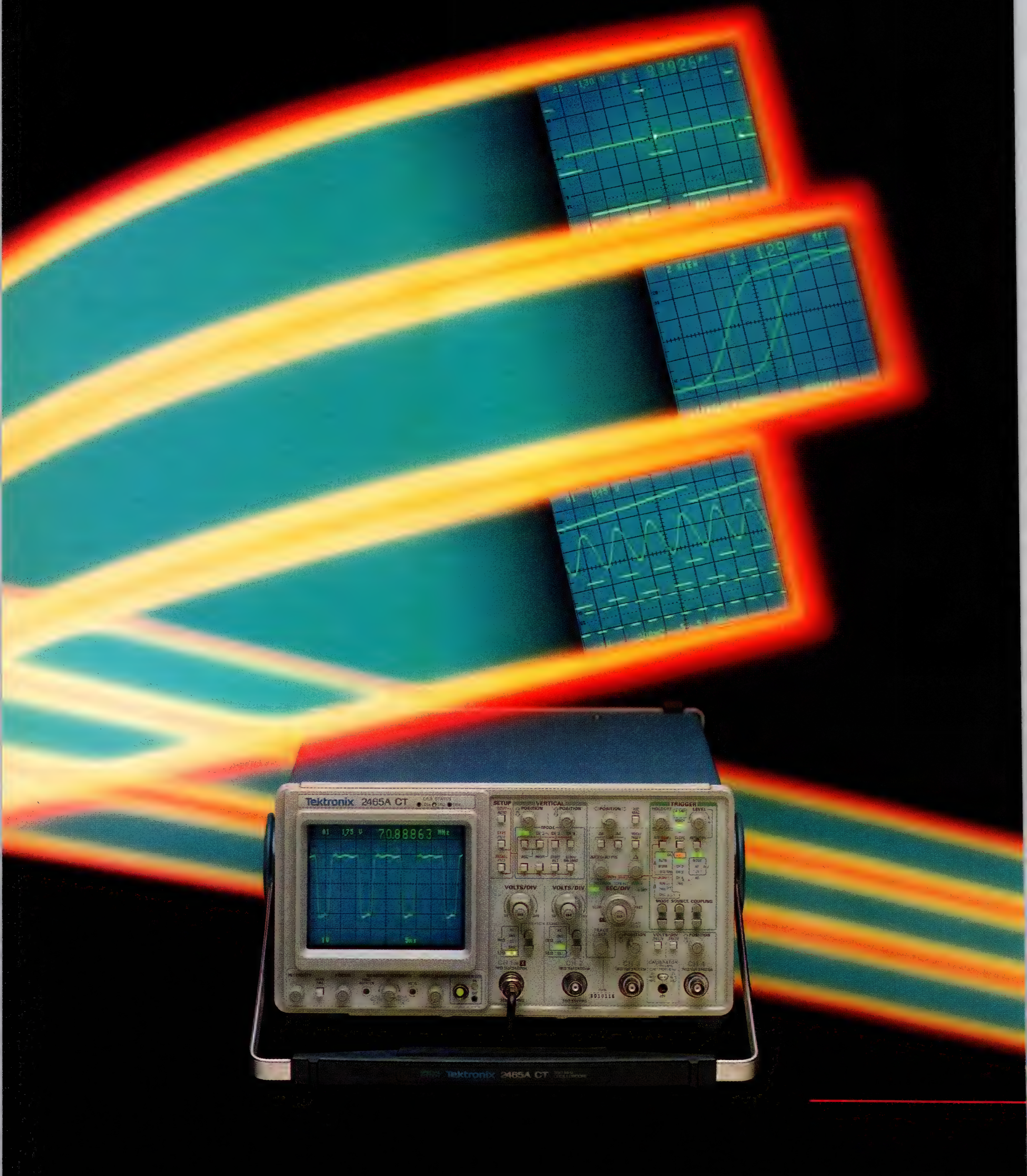
—Bill Travis

Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95052. Phone (408) 727-9222.

Circle No 729



Providing performance equivalent to that of a single OP-27, *the OP-470 from Precision Monolithics is the highest precision quad operational amplifier on the market. Its noise-to-*I_{CC} *performance ratio is the best of any available op amp, be it single, dual, or quad.*



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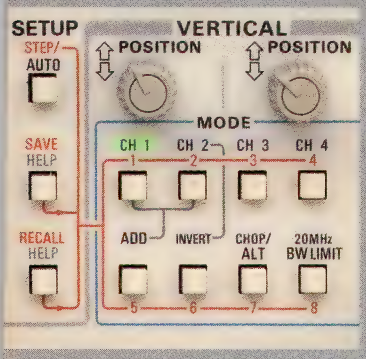
SEE. MEASURE. AUTOMATE. NOW AT THE TOUCH OF A BUTTON!

The Tektronix 2445A/2465A Family brings new convenience to leading-edge performance. Start with standards set by Tek's top portable analog scopes. Add new productivity-enhancing features for fast operation. And increase the 2465A bandwidth to 350 MHz.

The result: five new four-channel, dual time base oscilloscopes that bring unprecedented efficiency to your design lab, production line or field service site. You get high performance at its affordable best.



New AUTO-SETUP, SAVE/RECALL and SETUP SEQUENCING give the 2445A/2465A Family stand-alone automation—and enhance *your* productivity.

See your signals on screen in less time, automatically. Attach up to four probes to signal points, press AUTO-SETUP, and within seconds a stable, automatically triggered display of your probed waveform appears on screen for quick viewing or advanced parametric characterization.

Measure signal parameters more quickly with instant access to complex setups. The new SAVE/RECALL utility makes switching between measurements fast—just two buttons for a complete setup. And operator attention is focused on answers, not on control adjustments.

Non-volatile memory for 30 setups stores all front-panel information, including cursor locations and control settings for the extended measurement options. You can also store seven-character alphanumeric labels with each setup—as test titles or even operator prompts. HELP message makes operation even easier.

Automate repetitive measurement sequences without an external controller—and without writing a single line of code. Now set up, store and sequence systematic verification procedures for engineering prototypes, production test or field service without a computer. Using the STEP button or an external switch you can step through up to 30 setups in the order you choose.

Features	2465A	2445A
Probe Tip Bandwidth	350 MHz	150 MHz
No. of Input Channels	4	4
Channel 1/Channel 2 Vertical Sensitivity	2 mV/div to 5 V/div	2 mV/div to 5 V/div
Channel 1/Channel 2 Accuracy	2%	2%
Channel 1/Channel 2 Input Couplings	1MΩ: DC, AC and GND 50Ω: DC	
Max. Sweep Speed	500 psec	1 nsec
Max. Timing Accuracy	.55%	.55%
Trigger Frequency	500 MHz	250 MHz
Trigger Modes	Auto Level, Auto, Norm and Single Sequence	
Trigger Couplings	DC, AC, HF Reject, LF Reject and Noise Reject	

A wide range of vertical sensitivities and sweep speeds plus powerful triggering capabilities make it easy to study a tremendous variety of analog and digital signals. All with push-button convenience.

Included among 2400 Series standards are time and voltage cursors for immediate, effortless measurements. CRT readouts of waveform parameters and front-panel settings. Simplified trigger operation. All in a rugged, portable package backed by Tek's three-year warranty.

You can also choose among three specially configured packages: the 2465A CT, 2465A DM and 2465A DV. Designed especially for controller-based automation in specific application areas, the 2465A Special Editions combine multiple options into cost-effective measurement systems.

Or tailor the 2445A or 2465A to your needs with one or more measurement options: GPIB Interface, Digital Multimeter, Counter/Timer with enhanced triggering, 17-bit Word Recognizer and Video Measurement System.

For a closer look, call your Tek Sales Engineer for a demo today. For literature, or to find our sales office nearest you, call Tek direct:
Call toll-free
1-800-426-2200
In Oregon, call collect:
1-627-9000

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CIRCLE NO 138

XYCOM from HAMILTON/AVNET

Xycom, a manufacturer of industrial electronic products since 1969, now distributes its VMEbus boards through Hamilton/Avnet. So now, you get Hamilton/Avnet local service along with exciting advances from Xycom, including its new family of Single-High VME modules.

Half the size of previous Double-High Products, Xycom Single-High modules give you full VMEbus performance at STD bus prices. The selection includes a 68000 Processor board, a Memory board, and a Disk Control board as well as Digital In/Out, Analog In/Out, and Serial Communications boards.

And now you can get to know the Xycom line at a terrific savings! For each 68000 Processor module (XVME-600) shipped to you before the end of the year, you'll receive a $100 factory rebate off the already low price. So your final cost is less than half what you'd pay other sources!

Call us today or send in the coupon for more information on the complete Xycom Single-High and Double-High VMEbus product line. Talk to your local Hamilton/Avnet sales representative, or call toll-free: 1-800-4-HAMILTON (1-800-387-6979 in Canada, 1-800-387-6849 in Ontario and Quebec).

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The engineers and technicians at Computer Products Value Added C ter can configure your VME system your custom requirements, incluc integration of boards, mass stor enhancements and installation of operating system. Your system can delivered to you completely tested ready to run, so that you can conc trate on the work related to your part lar applications.

Our Value Added Center welcor your calls regarding integration Xycom products or any other VME syst enhancement. Call toll free at 1-8 228-7886 (U.S.) or 1-800-523-9811 (C fornia). For off-the-shelf orders, ple call our toll free number at left.

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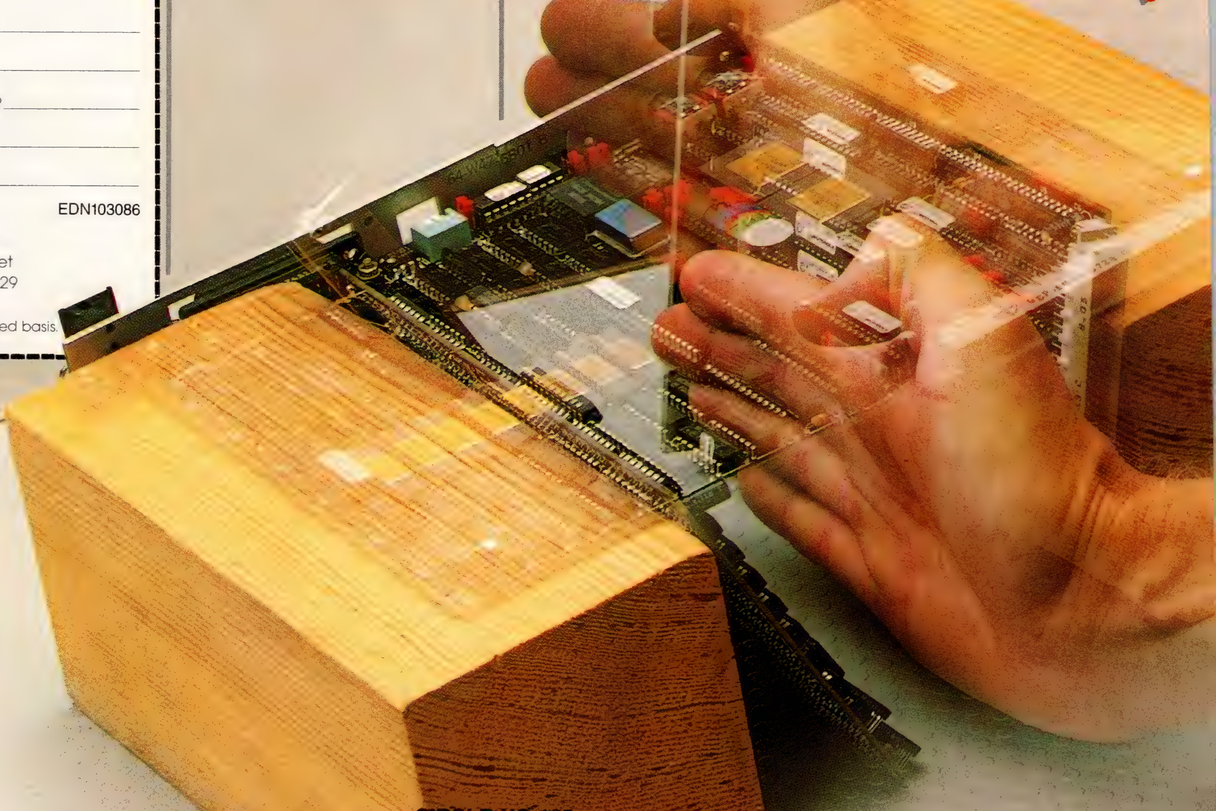
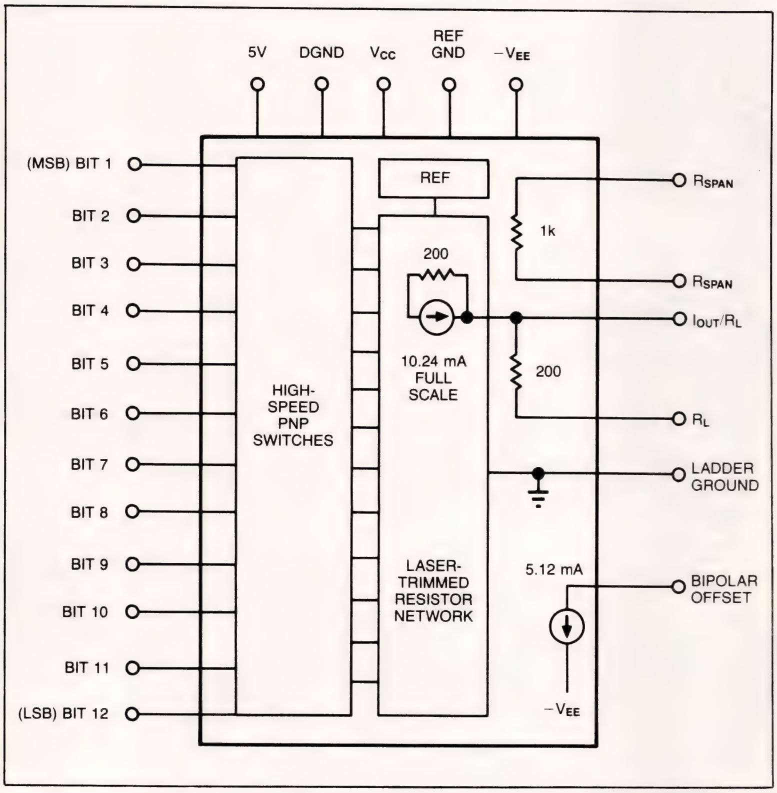
COMPUTER PRODUCTS DISTRIBUTION THROUGH A NATIONWIDE TECHNICAL NETWO



READERS' CHOICE

Of all the new products covered in EDN's **August 21, 1986,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **August 21, 1986,** issue.

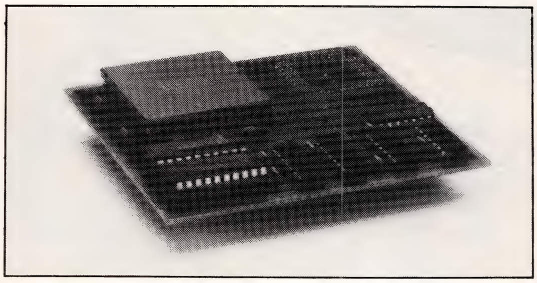


▲ D/A CONVERTER

The AD568 12-bit D/A converter is fabricated with a complementary bipolar process and offers a settling time of 50 nsec typ (pg 89).
Analog Devices Inc.
Circle No 601

PRESSURE SENSORS

The Nova-P Series TO-8 and TO-5 packaged silicon pressure sensors exhibit static accuracies of ±0.1% and operate over 0 to 70°C (pg 217).
NovaSensor.
Circle No 603



▲ TRANSLATOR

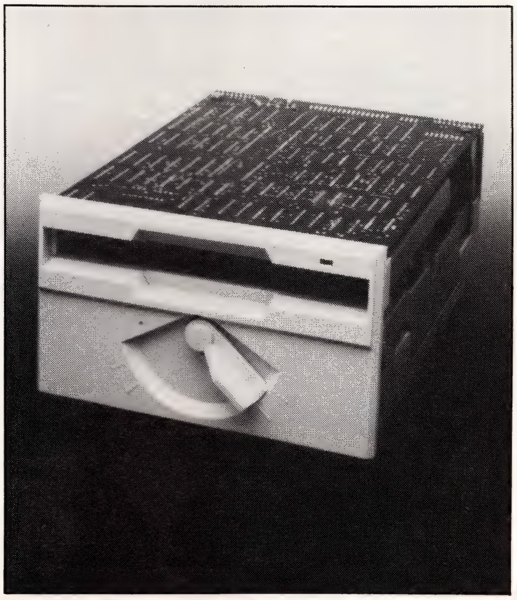
The 386 Translator transforms an IBM PC/AT or compatible computer into an 80386 programming environment (pg 232).
American Computer & Peripheral Inc.
Circle No 604

◀ DC/DC CONVERTERS

The PS-2805 and PS-2815 dc/dc hybrid converters have an efficiency rating of greater than 80% (pg 242).
Intech Inc.
Circle No 605

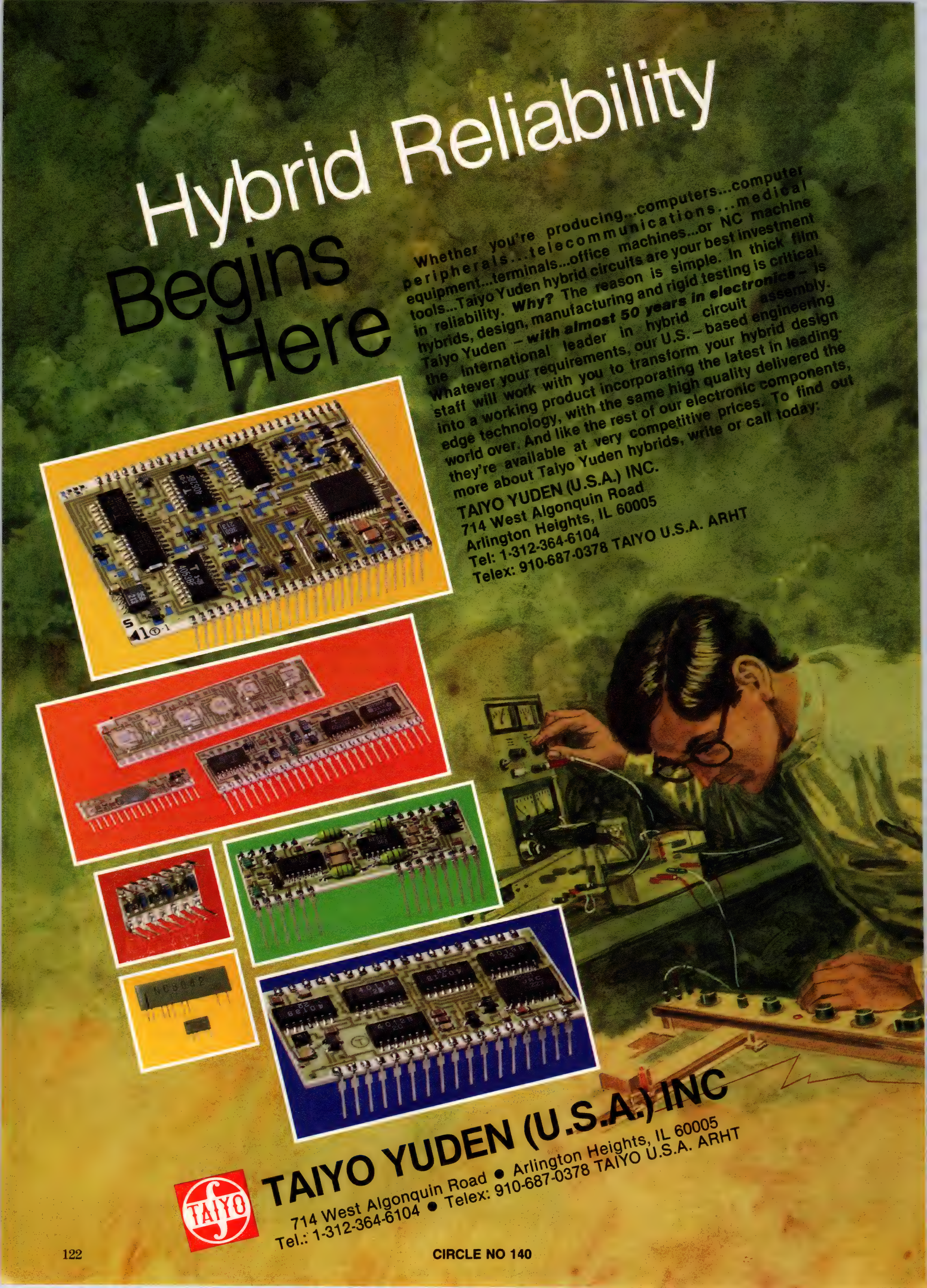
SCSI OPTICAL DRIVE ▶

The SCSI 5984 disk drive provides 200M bytes of storage area on each side of a removable, write-once optical disk (pg 206).
Optotech Inc.
Circle No 602



SYSTEM V FOR PC/AT

System V/AT is an adaptation of AT&T's Unix System V, Release 2 iAPX286 Version 1a; it turns a PC/AT or compatible computer into a multiuser, multitasking computer (pg 256).
Microport Systems.
Circle No 606



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Whether you're producing...computers...computer peripherals...telecommunications...medical equipment...terminals...office machines...or NC machine tools...Taiyo Yuden hybrid circuits are your best investment in reliability. ***Why?*** The reason is simple. In thick film hybrids, design, manufacturing and rigid testing is critical. Taiyo Yuden – ***with almost 50 years in electronics*** – is the international leader in hybrid circuit assembly. Whatever your requirements, our U.S. – based engineering staff will work with you to transform your hybrid design into a working product incorporating the latest in leading-edge technology, with the same high quality delivered the world over. And like the rest of our electronic components, they're available at very competitive prices. To find out more about Taiyo Yuden hybrids, write or call today:

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CIRCLE NO 140

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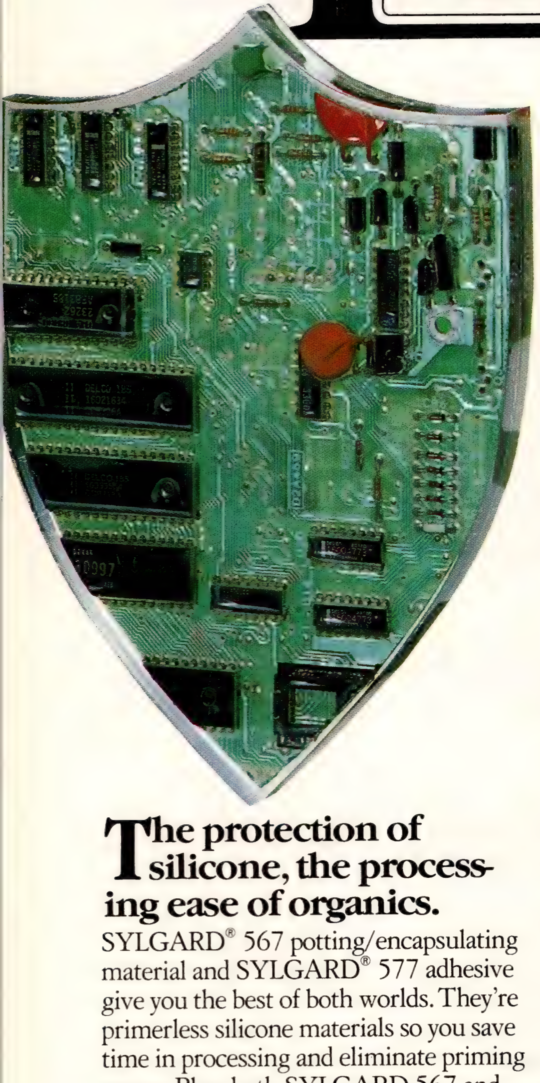
COMPUTERVISION

CIRCLE NO 143

Dow Corning Presents

The Guide to Total Electronics Protection



Your world is high-performance electronics. Our world is high-reliability protective materials. And whatever your needs are, we've got you covered. Here are a few examples:

The protection of silicone, the processing ease of organics.

SYLGARD® 567 potting/encapsulating material and SYLGARD® 577 adhesive give you the best of both worlds. They're primerless silicone materials so you save time in processing and eliminate priming errors. Plus, both SYLGARD 567 and 577 keep their elastomeric properties at −55°C and hold their physical performance properties at 200°C.

CIRCLE NO 102

Fast-cure coating for fiber optics.

OPTIGARD™ optical fiber coating UV-cures in just 0.3 seconds—5 to 20 times faster than thermal-curing coatings. And it protects against moisture and "microbends" better than acrylate coatings. It's part of the OPTIGARD family which includes fiber optics grade $SiCl_4$ core and cladding and OPTIGARD 5565 cable filler.

CIRCLE NO 103

New vacuum pump fluids perform. Cost less.

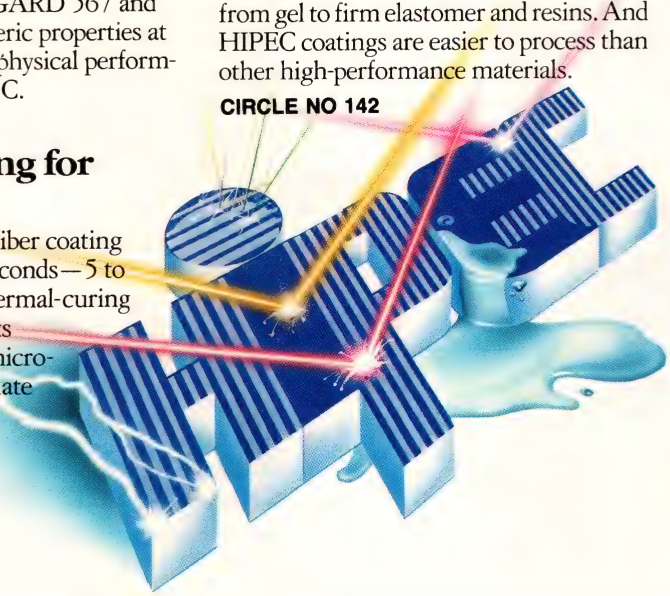
In semiconductor-vacuum applications, pump fluids have to stand up to corrosive gases, heat and pressure. Dow Corning® 711 mechanical pump fluid meets the test and costs less than other inert fluids.

CIRCLE NO 141

Life insurance for semiconductors.

Stress. Moisture. Ion contamination. Voltage leakage. Alpha particles. All are killers of your devices, robbers of reliability. Now you have a defense against them. HIPEC® coatings protect semiconductors and hybrids through a wide range of temperatures and environments. They're available in a variety of forms from gel to firm elastomer and resins. And HIPEC coatings are easier to process than other high-performance materials.

CIRCLE NO 142



Coating makes repairs on PC boards easier.

A PC board coating simply has to be reliable. And with DOW CORNING® 1-2577 conformal coating you get more: easy repairability when components need replacing. Add superior protection in extreme environments, versatile processing with dipping or spraying, and you have all the reasons major automotive and military electronics companies choose DOW CORNING 1-2577.

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There's more.

There's also our unique team of experts whose only mission is to develop and customize coatings, adhesives, dispersions, sealants, and components specifically for you. Supported by dedicated research and manufacturing facilities, we will help you meet tomorrow's challenges today. Ask about our Specialty Elastomers Group.

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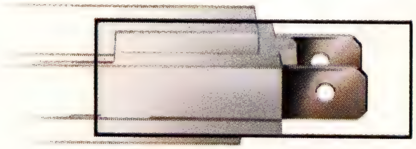
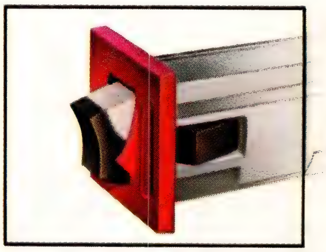
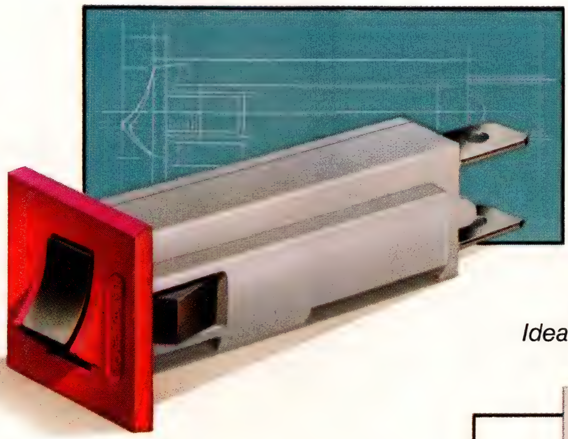


• *.250" quick-connect terminals make wiring easy.*

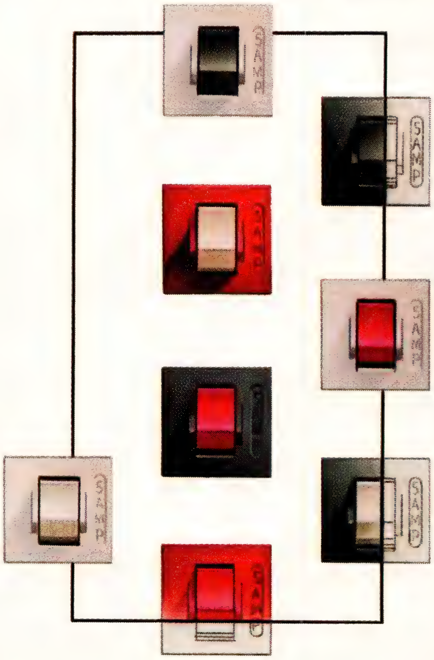
• *Trip indicator warns of a possible circuit problem. Choice of red or white.*



• *Special molded clips snap securely into standard ⅝" panel cutouts. No redesign or repunching.*



• *Variety of bezel and button colors permit color coding of circuits. Ideal for convenient up front control panel location.*



P&B's new snap-in circuit breakers end fuse replacement worries.

Our W28 series thermal circuit breakers fit the same cutout as many ⅝" fuseholders. And from 0.25 through 15 amps these UL recognized and CSA certified breakers do the same job as fuses. Only better. When the W28 trips, an indicator pops out to warn of a possible circuit problem. After the trouble is located and corrected, the W28 can be reset by simply pushing a button. But it can't be pulled out to disconnect the circuit.

Easy To Install. Wherever you presently use glass cartridge fuseholders, W28s can replace them without panel redesign or repunching. Think about putting them out front. That way they're easily accessible and their attractive appearance will add to your product's appeal. W28 breakers can be prewired and then snapped securely into the panel from the front.

Helps Sell Your Product. For everything from home entertainment equipment to medical instruments to industrial test gear, W28 breakers add selling points to your product. Good looks. The convenience of not searching for fuses. Protection against improper fuse rating substitutions. And they save the cost and trouble of maintaining a fuse inventory.

Write For Our Catalog. Find out about the economical W28 and our full line of magnetic and thermal circuit breakers. They're available off-the-shelf from authorized P&B distributors backed by our sizable factory inventory. Or contact your local P&B sales representative. Potter & Brumfield Inc., 200 South Richland Creek Drive, Princeton, Indiana 47671-0001. Call toll free **800/255-2550.**

8609

Potter & Brumfield A Siemens Company

CIRCLE NO 187

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average weeks	Last month's average weeks
TRANSFORMERS								
Toroidal	10	20	35	30	5	0	9.3	10.0
Pot-Core	0	28	39	28	5	0	9.6	9.4
Laminate (power)	20	25	40	10	5	0	6.6	8.3
CONNECTORS								
Military panel	0	10	50	20	10	10	13.1	10.6
Flat/Cable	22	37	33	8	0	0	4.6	5.6
Multipin circular	0	7	67	20	6	0	10.4	10.8
PC	20	30	35	15	0	0	5.8	7.9
RF/Coaxial	8	46	31	15	0	0	5.9	7.2
Socket	21	33	33	13	0	0	5.3	7.8
Terminal blocks	17	44	35	24	0	0	4.4	4.9
Edge card	14	19	52	10	5	0	7.3	6.3
Subminiature	13	37	38	6	6	0	6.4	8.4
Rack & panel	8	34	33	25	0	0	7.3	8.2
Power	7	53	27	7	6	0	6.0	7.1
PRINTED CIRCUIT BOARDS								
Single-sided	0	53	47	0	0	0	4.8	5.0
Double-sided	0	36	64	0	0	0	5.8	5.7
Multilayer	0	19	57	24	0	0	8.8	8.9
Prototype	3	81	16	0	0	0	2.9	3.6
RESISTORS								
Carbon film	39	33	20	8	0	0	3.6	3.8
Carbon composition	38	21	31	10	0	0	4.6	7.1
Metal film	21	49	24	6	0	0	3.9	5.9
Metal oxide	20	45	25	10	0	0	4.5	6.6
Wirewound	16	28	40	16	0	0	6.3	6.1
Potentiometers	14	27	43	16	0	0	6.6	7.9
Networks	18	25	32	21	0	4	7.6	7.5
FUSES	33	37	22	8	0	0	3.7	3.6
SWITCHES								
Pushbutton	14	43	32	11	0	0	5.1	5.1
Rotary	4	31	52	13	0	0	6.9	7.2
Rocker	17	28	44	11	0	0	5.9	7.3
Thumbwheel	7	14	57	22	0	0	8.3	11.3
Snap action	24	35	29	12	0	0	4.9	7.4
Momentary	11	50	33	6	0	0	4.6	6.9
Dual in-line	15	39	31	15	0	0	5.7	8.0
WIRE AND CABLE								
Coaxial	39	35	26	0	0	0	2.8	3.9
Flat ribbon	39	29	28	0	4	0	3.8	4.5
Multiconductor	32	41	23	0	4	0	3.8	5.1
Hookup	53	30	17	0	0	0	1.9	2.5
Wire wrap	40	35	20	5	0	0	3.1	3.9
Power cords	18	46	36	0	0	0	3.8	4.2
Other	30	10	30	30	0	0	7.4	8.3
POWER SUPPLIES								
Switching	0	31	35	30	4	0	9.4	9.3
Linear	5	33	38	19	5	0	8.0	9.1
CIRCUIT BREAKERS	13	39	26	18	4	0	6.8	9.3
HEAT SINKS	28	32	24	16	0	0	5.1	7.3

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average weeks	Last month's average weeks
RELAYS								
General purpose	22	26	37	11	4	0	6.2	6.5
PC board	17	33	29	17	4	0	6.8	7.7
Dry reed	10	40	20	20	10	0	8.2	10.5
Mercury	0	30	40	20	0	10	10.1	13.5
Solid state	13	25	31	25	0	6	8.9	8.9
DISCRETE SEMICONDUCTORS								
Diode	15	53	25	5	2	0	4.5	5.4
Zener	18	43	21	18	0	0	5.5	5.2
Thyristor	20	30	25	20	5	0	7.1	7.1
Small signal transistor	21	31	28	17	0	3	6.7	7.3
FET, MOS	5	30	40	20	0	5	8.6	7.7
Power, bipolar	5	43	33	14	0	5	7.3	8.1
INTEGRATED CIRCUITS, DIGITAL								
CMOS	11	33	28	25	3	0	7.6	7.5
TTL	14	24	41	17	4	0	7.5	8.1
LS	12	26	38	21	3	0	7.7	8.5
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	15	20	45	15	5	0	7.7	10.0
OP amplifier	17	20	27	30	3	3	9.2	8.8
Voltage regulator	19	22	28	28	0	3	8.2	6.6
MEMORY CIRCUITS								
RAM 16K	23	29	24	18	0	6	7.1	7.7
RAM 64K	32	24	24	16	0	4	6.2	6.9
RAM 256K	14	33	29	19	0	5	7.5	8.6
ROM/PROM	5	33	29	33	0	0	8.3	9.5
EPROM	16	37	17	27	0	3	7.4	8.4
EEPROM	5	16	37	37	0	5	10.8	10.8
DISPLAYS								
Panel meters	0	32	47	16	5	0	8.3	8.0
Fluorescent	0	30	30	30	10	0	10.4	10.4
Incandescent	0	40	30	10	20	0	10.0	12.7
LED	18	41	26	11	4	0	5.6	6.8
Liquid crystal	0	33	44	17	6	0	8.3	9.6
MICROPROCESSOR ICs								
8-bit	9	43	29	14	0	5	6.9	8.5
16-bit	5	48	28	14	0	5	7.0	8.4
FUNCTION PACKAGES								
Amplifier	12	44	19	19	0	6	7.3	10.7
Converter, analog to digital	3	27	53	10	3	4	8.3	10.7
Converter, digital to analog	6	29	29	24	6	6	10.1	10.8
LINE FILTERS	20	33	20	20	7	0	7.2	8.9
CAPACITORS								
Ceramic	26	34	20	20	0	0	5.5	6.0
Ceramic monolithic	23	27	35	15	0	0	5.8	7.4
Ceramic disc	31	24	31	10	4	0	5.5	7.4
Film	22	44	22	12	0	0	4.6	7.6
Electrolytic	10	31	47	9	3	0	6.7	7.1
Tantalum	18	24	49	6	3	0	6.1	7.8
INDUCTORS	5	38	28	24	5	0	8.1	9.3

Source: *Electronics Purchasing* magazine's survey of buyers

100% SOLUTIONS FOR 100-WATT APPLICATIONS.

ABBOTT'S COMPLETE LINE OF SINGLE AND TRIPLE OUTPUT 200 kHz SWITCHERS.

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DIMENSIONS	1.875″x4″x7.5″	1.875″x4″x7.5″	1.875″x4″x7.5″
INPUT	320-480 Hz	47-65 Hz	dc
	115V ac	115V ac	22-32V dc
	± 10%	± 10%	—
OUTPUT	100 watts	100 watts	100 watts
single	5,12,15,24,28V	5,12,15,24,28V	5,12,15,24,28V
triple	5± 12V or	5± 12V or	5± 12V
	5± 15V	5± 15V	5± 15V
SWITCHING FREQUENCY	200 kHz	200 kHz	200 kHz
EFFICIENCY	65%-80%	65%-80%	65%-80%
RIPPLE/NOISE	0.5%-2%	0.5%-2%	0.5%-2%
LINE & LOAD REGULATION	10 mV	10 mV	10 mV
EMI	MIL-STD-461B	MIL-STD-461B	MIL-STD-461B
ENVIRONMENT	MIL-STD-810C	MIL-STD-810C	MIL-STD-810C
	MIL-S-901C	MIL-S-901C	MIL-S-901C
INPUT PROTECTION	MIL-STD-704D	MIL-STD-1399	MIL-STD-704D
TEMPERATURE			
operating	−55°C to +100°C	−20°C to +71°C	−55°C to +100°C
storage	−65°C to +125°C	−55°C to +85°C	−65°C to +125°C
MTBF* (minimum—ground benign)	99,408 hours	97,935 hours	140,000 hours

*MIL-STD-217D (50°C baseplate)

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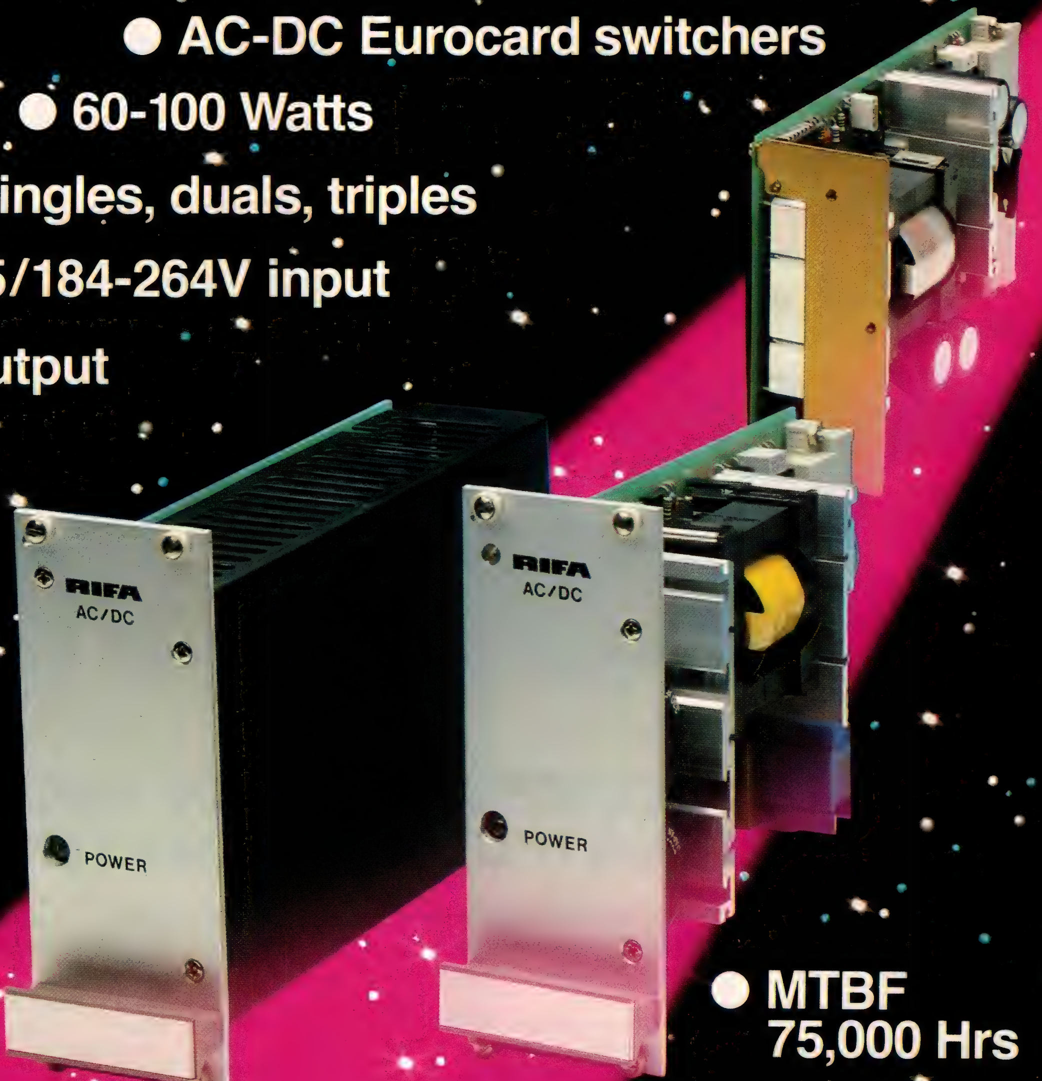

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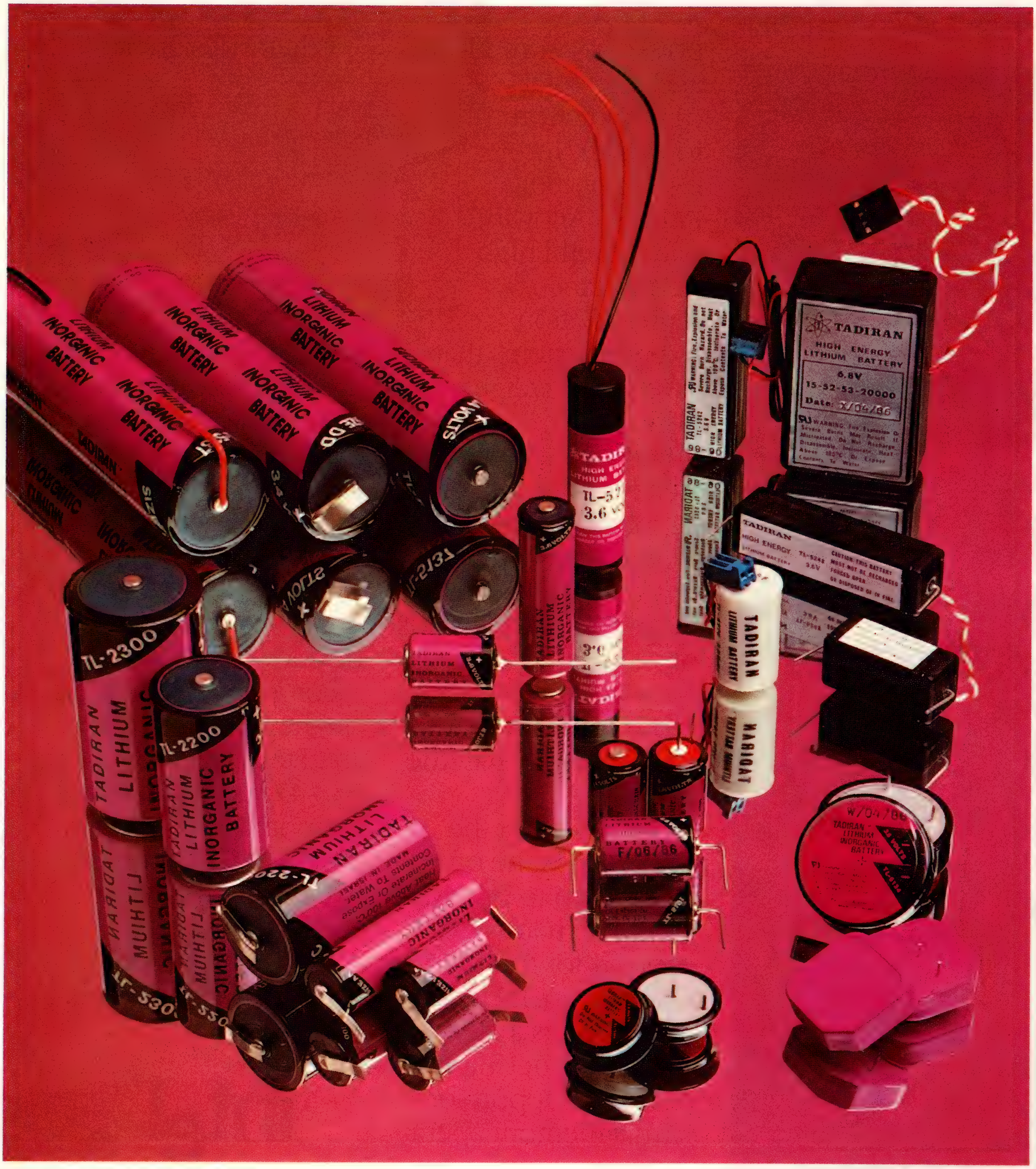
CIRCLE NO 158

Backup batteries



Batteries in a variety of chemistries *and packaging styles stand ready to provide backup power for electronic circuits. (Photo courtesy Tadiran)*

Battery makers are making steady improvements in both the chemistry and the mechanical construction of batteries. As a result, design engineers now have such a plethora of battery types to choose from that they can match virtually any application, no matter how big or how small, to an appropriate battery system.

Battery backup for electronics once meant using a small, pc-board-mounted battery to keep alive a real-time clock or a critical portion of memory during a power outage. Now, with low-power CMOS systems and improved batteries, designers face a wider span of backup capabilities, ranging from backing up the entire main dc bus of a system's switching power supply to powering just a single chip. You no longer have to limit your plans for battery backup to the absolute minimum critical circuitry that you want to keep alive; instead, you can consider backing up the optimal portion of your circuitry.

The need for backup power is almost as pervasive as electronics itself: Just walk through an average household after a brief power interruption, and virtually every room will have at least one electronic gadget flashing a reset message because it lacks a keep-alive battery. Similarly, critical computer-controlled equipment in military systems and in factories cannot simply reset and restart their programs after a power interruption. A robot, for example, might be in the middle of extracting a hot casting from a molding machine; without battery backup, rebooting the robot's control program might cause the robot to drop the casting and return its arm to a rest position.

Indeed, the versatility of the batteries available today is such that the distinction between backup and primary power is blurry for many applications. Consider, for example, a common lap computer like the Radio Shack Model 100. If someone asked you if the computer's NiCd battery was primary or backup power, you could argue that it was backup power because it keeps the computer's memory alive and intact after you switch off the machine; or, you could reason that it's primary power because the computer can operate directly from it. Actually, the Model 100's battery is both a backup and primary power source.

Silver, mercury, zinc air, alkaline (manganese dioxide), and carbon zinc (also known as Le Clanche) batteries are often used for primary power in consumer goods **(Table 1)**; electronic design engineers generally choose a backup battery from lead acid, nickel cadmium (NiCd), and lithium (Li) chemistries.

Selecting a battery type is akin to taking a shot at a moving target. Although batteries have been around since Volta first made a dead frog's leg twitch, progress and development of new products has been continuous. Improvement has come from two areas: packaging and chemistry.

Packaging innovations include the so-called paper batteries; versions from Seiko Instruments and Panasonic are less than 0.02 in. thick. You can expect even more exotic types of thin batteries in the future. Battery makers are reportedly readying lithium cells that you'll be able to permanently bend to conform to your packaging requirements. The bendable cells will be encased in steel; other packaging options include plastic: Renata offers a lithium cell encapsulated, along with isolation diodes, in plastic. Rayovac offers plastic-encapsulated lithium coin cells, as does Saft America.

Refinements to lead acid battery

In terms of chemistry, even the venerable lead acid battery has benefited from improvements in design. Whereas in the past battery makers optimized lead acid batteries for either float or deep-discharge applications, recent developments in starved-electrolyte chemistry have yielded sealed lead acid batteries that suit both float and deep-cycle applications. Two types of starved-electrolyte batteries are on the market: The original gelled-electrolyte cell has its acid electrolyte absorbed in a silica gel, and the more recent recombining lead acid battery has its acid electrolyte absorbed in a fiber-glass separator. Both battery types are sealed, require no water during their lifetimes, and vent gases from built-in pressure-relief valves only upon extreme overcharge.

Of the three most popular battery types—nickel cadmium, lithium, and lead acid—lead acid batteries are the least expensive for a given number of ampere-hours (Ahr). These batteries range in capacity from 1.0

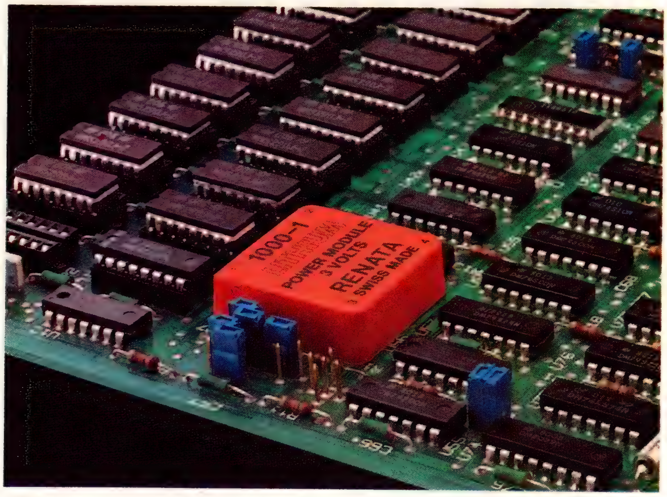
Charles H Small, *Associate Editor*

Rechargeable batteries typically require that you put 20% to 40% more energy into them than you remove during discharge.

TABLE 1—PRIMARY CELLS (EXCLUDING LITHIUM TYPES)

BATTERY TYPE	GENERAL CHARACTERISTICS (UNDER OPTIMUM OPERATING CONDITIONS)	CONFIGURATIONS AND RATED CAPACITY	NOMINAL CELL VOLTAGE	ENERGY DENSITY		SHELF LIFE (% LOSS/YEAR @70ºF)	TYPICAL OPERATING TEMPERATURE
				WEIGHT (Whr/lb)	VOLUME (Whr/in³)		
ALKALINE MANGANESE DIOXIDE (Zn/MnO_2)	POPULAR, GENERAL-PURPOSE PREMIUM BATTERY; GOOD LOW TEMPERATURE AND HIGH DISCHARGE-RATE PERFORMANCE; GOOD SHELF LIFE; SLOPING DISCHARGE CHARACTERISTIC	CYLINDRICAL CELLS TO 20 Ahr; ALSO AVAILABLE IN BUTTON CELLS	1.5	BUTTON: 25 CYLINDRICAL: 60	 2.4 5.2	5%	−4 TO +130ºF
MERCURIC OXIDE (Zn/HgO)	HIGH VOLUMETRIC CAPACITY; GOOD SHELF LIFE; FLAT DISCHARGE CHARACTERISTIC	BUTTON AND CYLINDRICAL CELLS FROM 40 mAhr TO 13 Ahr; ALSO AVAILABLE IN SPECIAL LARGER SIZES	1.35 OR 1.40	BUTTON: 50 CYLINDRICAL: 55	 7.3 7.4	4%	15 TO 130ºF
SILVER OXIDE (Zn/Ag_2O)	HIGH GRAVIMETRIC CAPACITY; GOOD SHELF LIFE: FLAT DISCHARGE CHARACTERISTIC	BUTTON CELLS TO 180 mAhr FOR SPECIALIZED APPLICATIONS	1.5	BUTTON: 60	 8.2	6%	−4 TO +130ºF
ZINC AIR (Zn/O_2)	HIGHEST ENERGY DENSITY ON CONTINUOUS DISCHARGE; EXCELLENT SHELF LIFE (UNACTIVATED); LIMITED DISCHARGE-RATE CAPABILITY AND SHELF LIFE WHEN ACTIVATED; FLAT DISCHARGE CHARACTERISTIC	BUTTON CELLS TO 1150 mAhr; LARGER CELLS TO 6.5 Ahr	1.4	BUTTON: 140	 19.0	2% (UNACTIVATED)	32 TO 122ºF

(SOURCE: EVEREADY)



This encapsulated lithium coin cell, *the 1000-1 from International Power Sources/Renata, features a built-in isolation-diode network.*

to 100 Ahr. Unfortunately, because lead acid cells don't come in button, coin, AA, C, D, and 9V transistor-battery sizes, they presently suit only higher-power applications. Smaller lead acid batteries should debut soon, however. Nickel cadmium batteries span 1.0 mAhr to 10 Ahr; that is, they overlap both lead acid types (on the high-power end of the spectrum) and lithium batteries (on the micropower end).

A lead acid battery delivers 2V/cell vs a NiCd's 1.2V/cell. A 6V application would require either five NiCd cells or three lead acid cells. All other factors being equal, the fewer the cells and interconnections your design has, the better it is.

Lead acid batteries carry weight

Where space and weight are not critical, and particularly in those applications where you require high current (2.0 Ahr or more,) sealed lead acid batteries are a good choice because of their lower initial cost. For example, a 6V, 4.4-Ahr NiCd battery sells for almost four times the price of a 6V, 5.5-Ahr sealed lead acid battery. Beyond 6 Ahr, the sealed lead acid battery tends to be the best choice.

Battery life for nonrechargeable (primary) batteries is a complex function of ambient temperature and discharge rate. For rechargeable batteries, additional factors intrude: the rate of charging and discharging, the depth of discharge, the number of charge-discharge cycles, and the amount of overcharging. For example, an Eagle-Picher lead acid battery will last for 2000 cycles to 20% depth of discharge, but for only 500 cycles to 50% depth.

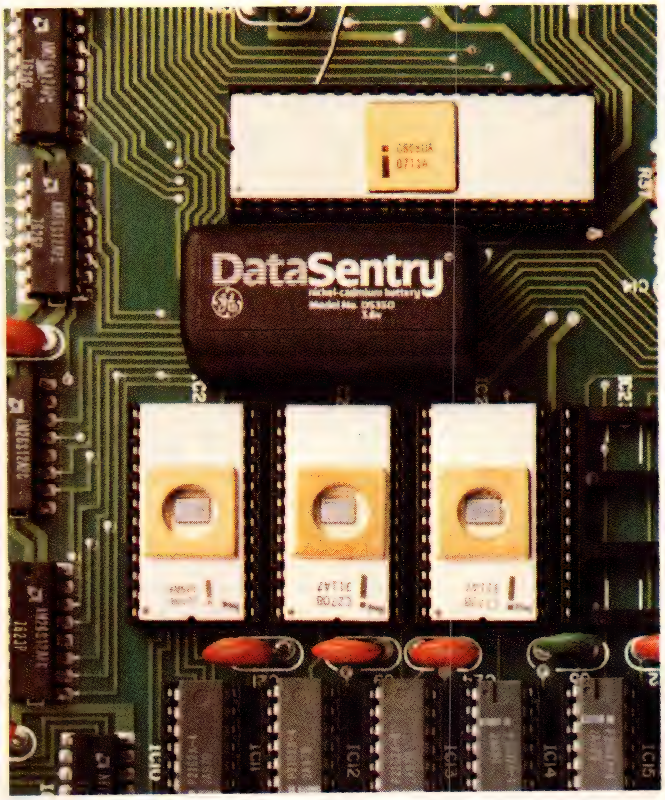
TABLE 2—RECHARGEABLE SEALED BATTERIES

BATTERY TYPE	VOLTS/CELL	ELECTROLYTE	GRID	FLOAT SERVICE LIFE (YEARS)	FLOAT CHARGE METHOD	CYCLIC SERVICE LIFE (CYCLES) 100% DISCHARGE	CYCLE CHARGING METHOD	STORAGE LIFE BETWEEN CHARGES	DISCHARGE PERFORMANCE OVER TEMPERATURE
SEALED NICKEL CADMIUM	1.2	STARVED RECOMBINING	NA	4 TO 8	CONSTANT CURRENT	500	CONSTANT CURRENT OR FAST CHARGE	2 TO 3 MONTHS	GOOD AT HIGH RATES AND LOW TEMPERATURE
GELLED/ ABSORBED ELECTROLYTE LEAD ACID	2.0	GELLED	LEAD CALCIUM	2 TO 10	CONSTANT VOLTAGE	100 TO 200	CONSTANT VOLTAGE (CURRENT LIMITED)	6 MONTHS TO 1 YEAR	GOOD AT HIGH TEMPERATURE AND LOW RATES
SEALED RECOMBINING LEAD ACID	2.0	STARVED RECOMBINING	PURE LEAD	6 TO 10	CONSTANT VOLTAGE OR CONSTANT CURRENT OR 2-STEP	200+	CONSTANT VOLTAGE OR FAST CHARGE	3 YEARS	GOOD AT HIGH TEMPERATURE AND HIGH RATES

Because manufacturers cannot test all batteries for all possible operating conditions, a typical battery specification will cover only typical applications. Some battery manufacturers attempt to specify some minimum life at certain charging rates and ambient temperatures, whereas others measure life in terms of charge/discharge cycles, specifying the charge/discharge rates, and depth of discharge.

It's important to keep in mind impedance as well. Most engineers think of batteries as little more than a source of EMF and as possessing no other electrical properties than their voltage and internal resistance. But batteries do have a complex impedance that can have a marked effect on a circuit—particularly high-speed switching circuits. Inexplicably, battery manufacturers generally don't know the impedance of their products. To measure the complex impedance of a battery, you'll need a high-power ac bridge or an FFT impedance analyzer. If you don't have access to either of those, you can turn to the Battery Technology Center of the Mellon Institute (Pittsburg, PA). The center can provide impedance for certain batteries or will measure it for you.

For typical duties where the batteries are repeatedly charged and discharged, battery makers express battery life in cycles; where batteries are on continuous charge with only occasional discharges, manufacturers



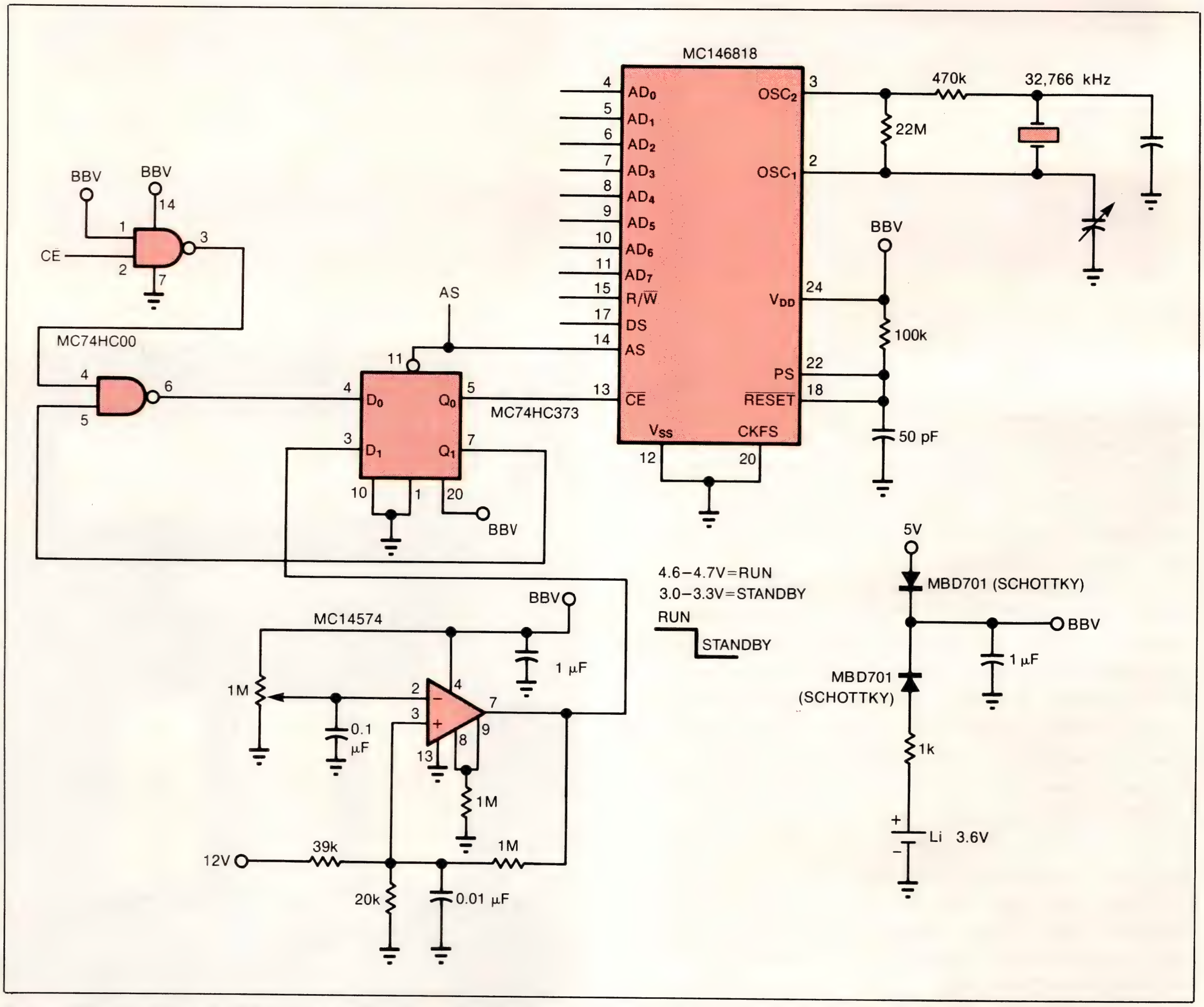
***Rechargeable NiCd batteries** in the Data Sentry Series from General Electric provide as many as 500 deep-discharge cycles.*

Some designers are unaware that certain batteries aren't UL certified for user replacement.

express life in years. A major factor affecting cycle life is the extent to which you discharge the battery in each cycle. For continuous duty, the major determining factor in battery life is the temperature of the batteries when on continuous charge. Most battery literature shows battery capacity under continuous load. But some cells—manganese dioxide lithium cells, for example—last much longer under pulse-load conditions.

If your application dictates the need for rechargeable batteries, you'll have to analyze duty cycle, cycle life, reliability, and storage life (in addition to the capacity your application requires). If the equipment in your application will undergo many charge/discharge cycles, NiCd batteries may be the best choice from among the three types of rechargeable batteries because they deliver 500 or more charge cycles (to 80% of capacity) **(Table 2).**

Unfortunately, NiCd batteries do have a couple of potential disadvantages when compared with lead acid batteries. Certain NiCd types suffer from a phenomenon called memory effect. Some applications require that a battery undergo short, repetitive periods of use,



A careful reading of the MC146818 µP's *data sheet led a Tadiran application engineer to add the external latches for AS and $\overline{CE}$ to his backup-battery circuitry because these functions do not work properly at standby voltage levels. Similarly, designers should take steps to decouple critical memory from spurious activity on address and data lines during a µP's power-down/power-up cycle. The improved MC146818A does not require the external latches.*

Voltage detector backs up backup battery

Even if you've selected the battery with the longest shelf life, largest capacity for its size, and greatest number of recharge cycles, when it's under load, that battery has only so many ampere-hours in it: When the juice stops flowing, your circuit dies.

Some makers tout a flat voltage-vs-time discharge curve as an advantage. A flat curve is an advantage if you want your battery to function as a well-regulated power supply. But, a flat curve also means you can't tell a nearly dead battery from a fresh one.

If the battery you select exhibits a fall off of voltage with loss of capacity, you can employ a simple voltage detector IC or design your own circuit. Intersil (Cupertino, CA) and Maxim (Sunnyvale, CA) make the 7665 low-power under/overvoltage detector IC. The chip contains two individually programmable voltage detectors; it was designed specifically for battery-powered applications and consumes 3 μA over its 1.6 to 16V operating range. The device's output transistors can sink as much as 20 mA.

Under low drain conditions, your battery may not exhibit sufficient voltage drop with capacity loss for you to be sure that a voltage drop isn't caused by random temperature changes. In cases like this, you may have to periodically draw short pulses of current from the battery and measure its voltage drop under load. If you can arrange to store the pulses in a capacitor, your circuit can conserve power while providing an alarm.

Smoke detector example

The circuit in **Fig A** comes from US Patent 3,778,800, granted to BRK Electronics (Aurora, IL), the maker of First Alert smoke detectors, and provides an example of a simple low-battery alarm that doesn't use an IC. (The company has since re-engineered its smoke-detector electronics into a custom IC.)

The ion-chamber smoke detector, in clear air, draws sufficient current to hold FET Q_1 on. In the presence of smoke, its resistance increases, eventually turning Q_1 off. With Q_1 off, Q_3 switches on SCR D_1, which sounds the alarm. Capacitor C_1 provides feedback to transistor Q_2 and initially ensures that transistor Q_1 switches off.

When C_1 discharges completely, it disturbs the bias on Q_1 via Q_2 and causes Q_1 to turn on again, which interrupts the alarm and turns off Q_3. If the ion chamber still contains smoke, Q_1 will turn off again after C_1 charges up again through resistors R_7, R_8, and R_9. Thus, the smoke detector emits a series of alarm signals when it detects smoke.

Notice, though, that transistor Q_2 also senses the battery voltage via the resistive divider formed by R_6 and R_7. If the battery voltage falls, Q_2 will turn off and trigger the alarm. In this case, the low-voltage condition only turns Q_2 partially off, which causes the alarm to sound a series of short, intermittent alarm signals as opposed to the rapid, increasingly insistent smoke alarm.

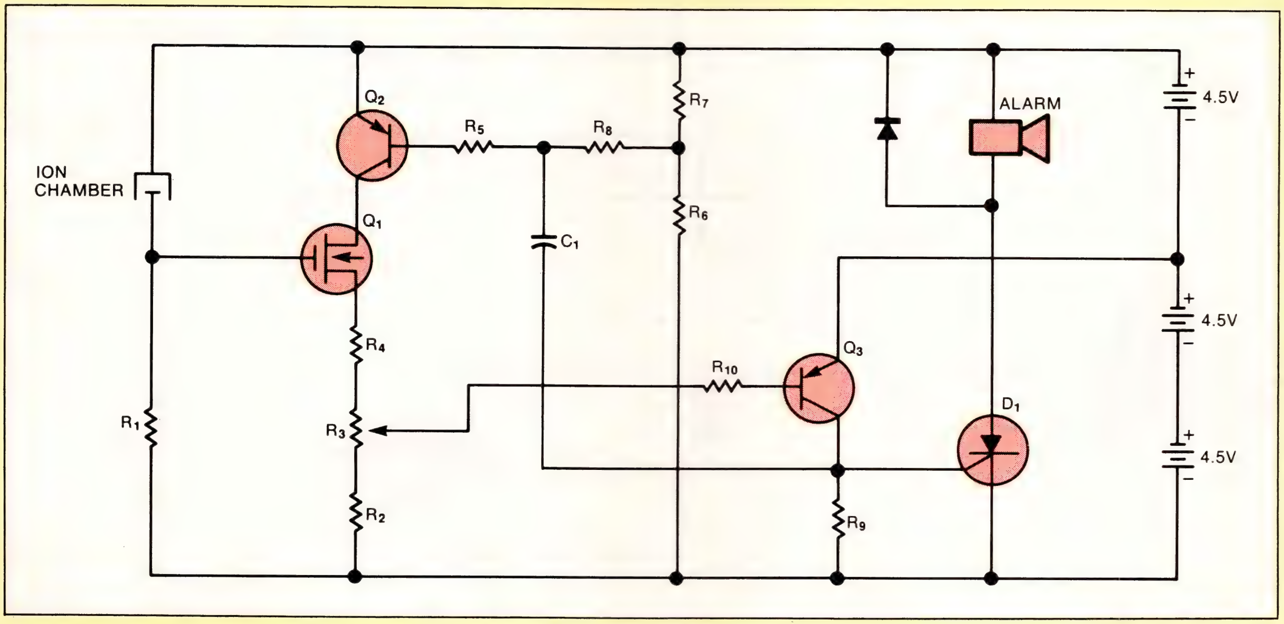


Fig A—a simple, but patented, circuit provides a smoke detector *with an alarm for both smoke and low batteries. The R_6/R_7 voltage divider monitors the battery and will turn Q_2 off, and Q_1 as well, when the battery voltage falls too low. The smoke-detector chamber will also cut Q_1 off when it senses smoke. Q_1, via Q_3, triggers SCR D_1 and sounds the alarm. Capacitor C_1 provides feedback that causes the alarm to sound intermittently. The smoke detector and low-battery circuits sound the alarm at two different rates.*

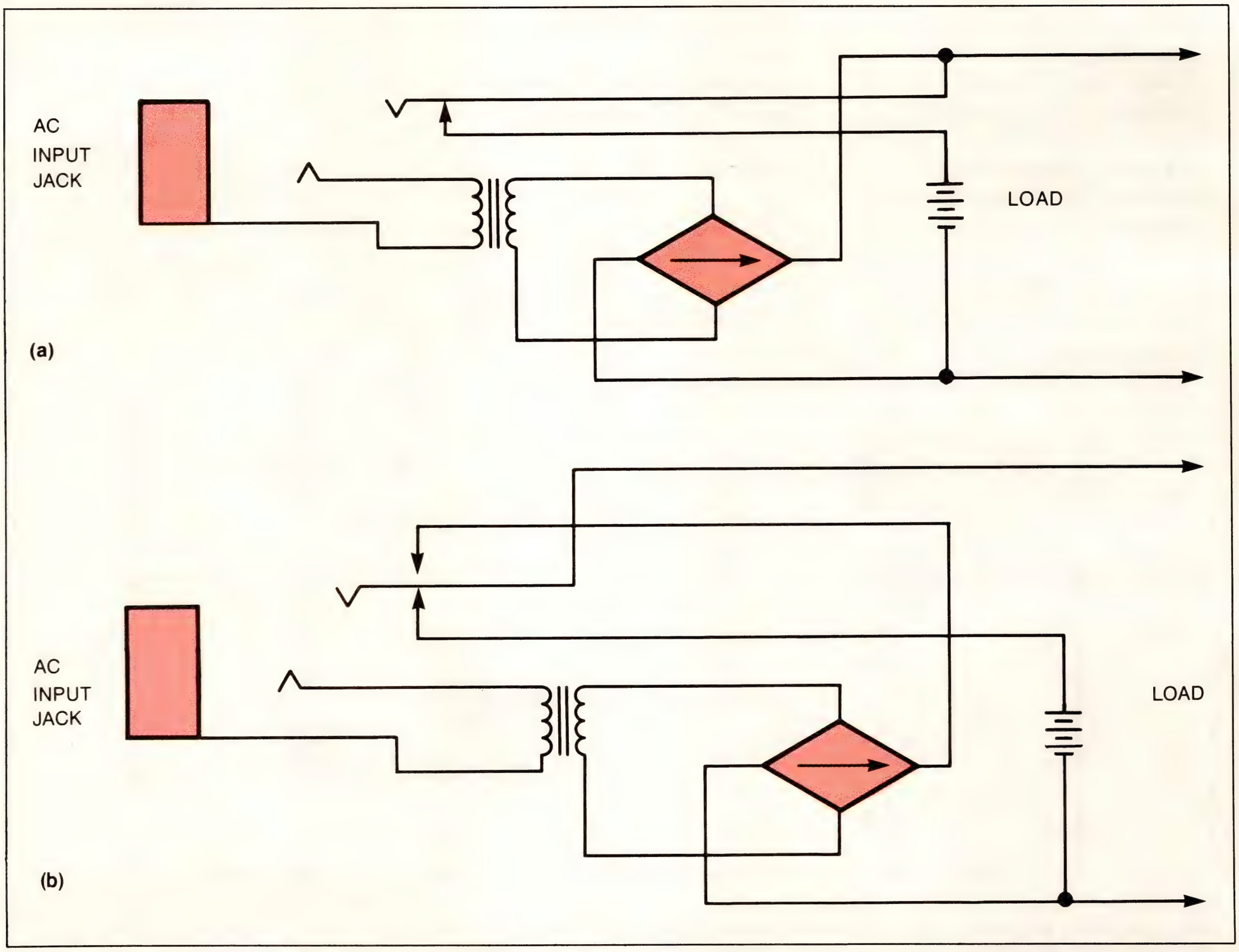
You shouldn't use your ICs' worst-case specs to size your battery without first determining the ambient temperature of the ICs.

which consume only a small portion of the battery's total capacity. Under these cyclical conditions, some NiCds forget their actual capacity and become conditioned to deliver only the small amount of power normally required.

Not all NiCd batteries are affected this way, though. Panasonic, for example, claims that its NiCd batteries are immune to the memory effect. Varta also claims that the mass-plate construction of its NiCd cells virtually eliminates it. In any case, two or three deep-discharge cycles usually eliminates the problem.

If you ascertain that your application doesn't really call for such a large number of charge/discharge cycles, a recombining lead acid battery will deliver 200 cycles at 100% depth of discharge. For discharges to less than 100%, a recombining battery delivers 600 cycles at 60% depth of discharge before falling below 80% of its rated capacity. Depending on the source you consult, gelled electrolyte batteries will either deliver 100 to 150 cycles at 100% discharge to 50% of rated capacity or are capable of 200 to 500 deep discharges.

Gelled-electrolyte and recombining lead acid batteries generally do not perform well in portable applications because of their poor low-temperature performance and short cycle life at high depths of discharge. Some standard lead acid batteries drop to 20% of rated capacity at −40°C, and recombining lead acid batteries will drop to 50% of capacity at these same low tempera-



Panasonic recommends design techniques *to protect primary backup batteries from recharging during application of ac power. The circuit in* ***a*** *can result in the battery being connected to the rectified ac input if the user pushes the ac adapter's plug in halfway. The better circuit in* ***b*** *disconnects the battery before connecting rectified ac power to the load.*

tures. Further, one Renata battery's self-discharge rate rises from 1% per year at 20°C to 1% per month at 60°C. Failure to plan for a drop in capacity at extreme temperatures will come back to haunt the careless designer.

If your application more closely resembles float rather than cyclic duty (as many do) and sits on charge 90 to 95% of the time, NiCd may not be the optimum choice. A NiCd battery's life is five to seven years; a sealed, recombining lead acid battery retains 80% of its capacity after eight to 10 years of service. In comparison, some standard lead acid units have an expected life of two to five years before their capacity drops to 50% of rated capacity.

Backup batteries span a wide range of chemistries. *These lithium batteries and cells from Saft are available in the following chemistries: thionyl chloride, manganese dioxide, copper oxide, copper oxyphosphate, and sulfur dioxide.*

Moreover, sealed lead acid batteries that exhibit extended life are also available. Yuasa Battery offers 12 and 6V versions rated for a 10-year life. According to Johnson Controls' Globe Battery Div, gelled-electrolyte lead acid batteries actually increase in capacity during the early stages of their lives. Such batteries will also gain in capacity slightly while on extended charge such as in float service where discharges are infrequent.

As far as reliability goes, a NiCd battery often fails because of its separator, particularly when the cells experience high temperature. Consequently, manufacturers offer special high-temperature cells that typically have a polypropylene separator. Although giving longer life and improved performance at higher temperatures, they give somewhat lower performance at cooler temperatures.

Similarly, recombining lead acid batteries can form dendrites, which can penetrate the separators and produce internal short circuits. Some manufacturers use a separate rigid polymer separator that prevents

Selection guide identifies criteria

Electrochem Industries recommends that a designer ask himself the following questions before deciding which battery suits his application. (The company, upon request, will supply a form with these questions. If you fill it out and send it in, the company will return a recommendation within a week.)

- What voltage do you need: maximum, minimum, cutoff (V)?
- What capacity are you looking for (Ahr)?
- If you need continuous operation, what current level do you need: average, peak, for how long (A)?
- If you need intermittent operation, what duty cycle do you need: on-time, off-time, current, background current, number of cycles?
- What operating temperature range do you require: maximum, minimum, average?
- If your application requires a pack of cells, how do you want it encased: shrink wrap, molded case, other?
- For storage and standby, what temperature range do you require: maximum, minimum (°C), storage interval?
- What is the size and shape of your battery compartment?
- What is the maximum weight allowed?
- For terminals, what type do you need: solder tabs, terminal caps, axial leads, pc-board leads, other?

For every 10° C drop in temperature, the keep-alive current a chip draws will drop by 50%.

shorts. The separator can raise the battery's internal resistance slightly. Gelled-electrolyte lead acid batteries normally use the polymer separator and therefore don't suffer short circuits.

The rechargeable battery types react differently to being recharged after being allowed to self-discharge. A NiCd battery will recover even after three to five years of storage. You can store a recombining lead acid battery for three years, whereas a gelled cell requires charging every six months or it will suffer permanent damage. It's wise to keep in mind that a NiCd battery must be charged continuously. If you leave a NiCd battery uncharged, it will lose 1% of its capacity daily; in contrast, a sealed lead acid unit loses only 1% of its capacity per week.

For low-current, pc-board-mounted backup batteries, lithium batteries may well be more suitable than NiCds (although the much-cheaper alkaline button cells suit some applications, too). Lithium cells offer the following advantages over NiCd batteries: They don't require a charging circuit, they have a long shelf life, and they have high enough output voltage to provide standby power to CMOS circuits from a single cell. Note that, in the case of batteries generally, increased capacity costs far less than increased voltage: Doubling capacity by going to a larger cell costs less than doubling voltage by connecting two cells in series.

Once you decide upon lithium, you still have to decide which type of lithium battery best suits your needs, and this can be particularly confusing. Over 20 lithium makers are selling an equal number of different chemistries, encased in at least three different packaging styles. The anodic chemical reaction with the lithium within a cell provides only a portion of the cell's voltage—the reaction at the cathode provides the remainder. Because differing cells use different materials for their cathodes and electrolytes, lithium cells exhibit a range of operating temperatures, open-circuit voltages, and current-sourcing capabilities.

Although you can obtain lithium cells in capacities ranging from milliampere-hours to over 20,000 Ahr, lithium batteries are now economical only for micropower loads. However, Kodak's entry into the over-the-counter battery market with 9V and AA batteries may signal a further encroachment of lithium batteries into NiCd territory. Note that Kodak's new line of 9V transistor batteries have gold-plated contacts to ensure that the company's batteries will still have low-resistance connections with the passage of time—something you may not get if you plug your pc-board-mounted lithium cells into battery holders rather than solder them in.

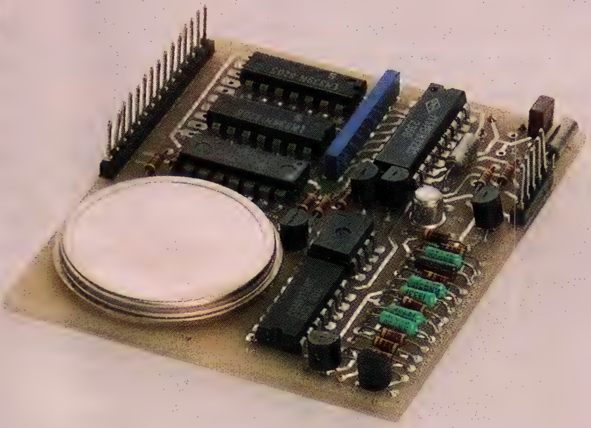
You can classify lithium cells into categories by the type of cathode and electrolyte they use: soluble cathodes, solid cathodes, and solid electrolytes. (**Table 3** lists the features of the three categories; **Table 4** details

TABLE 3—LITHIUM CELL TYPES

TYPE OF CELL	ELECTROLYTE	POWER CAPABILITY	SIZE (Ahr)	OPERATING RANGE (°C)	SHELF LIFE (YEARS)	CATHODES	NOMINAL CELL VOLTAGE (V)	COMMENTS
SOLUBLE CATHODE (LIQUID OR GAS)	ORGANIC OR INORGANIC (W/SOLUTE)	MODERATE TO HIGH POWER, W	0.5 TO 20,000	–55 TO +70	5 TO 10	SO_2 $SOCl_2$ SO_2Cl_2	3.0 3.6 3.9	HIGH ENERGY OUTPUT, HIGH POWER OUTPUT, LOW TEMPERATURE OPERATION, LONG SHELF LIFE, MIL SPEC
SOLID CATHODE	ORGANIC (W/SOLUTE)	LOW TO MODERATE POWER, mW	0.03 TO 5	–40 TO +50	5 TO 8	V_2O_5 CrO_X Ag_2CrO_4 MnO_2 $(CF)_N$ S CuS FeS_2 FeS CuO $Bi_2Pb_2O_5$ Bi_2O_3	3.3 3.3 3.1 3.0 2.6 2.2 1.7 1.6 1.5 1.5 1.5 1.5	HIGH ENERGY OUTPUT FOR MODERATE POWER REQUIREMENTS, NON-PRESSURIZED CELLS
SOLID ELECTROLYTE	SOLID STATE	VERY LOW POWER, µW	0.003 TO 0.5	0 TO 100	10 TO 25	$PbI_2/PbS/Pb$ I_2 (P2VP)	1.9 2.8	EXCELLENT SHELF LIFE, SOLID STATE—NO LEAKAGE, LONG-TERM MICROAMPERE DISCHARGE

(SOURCE: THE HANDBOOK OF BATTERIES AND FUEL CELLS (REF 1))

Remember when backup battery assembly was like putting a round peg in a square hole?



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CIRCLE NO 150

The distinction between backup and primary power is now blurry for many applications.

the characteristics of the solid-cathode chemistries.) Soluble cathodes are generally manufactured in cylindrical configurations in sizes to 25 Ahr. Unfortunately, because cylindrical cells have more effective surface area than button or coin cells, they have a higher self-discharge rate.

The nonaqueous chemistries, in addition to their lower self-discharge, present other advantages over aqueous systems. These advantages, which satisfy the needs of some military and consumer applications, include higher energy densities, hermetic-sealing possibilities, a choice of output voltages, and broader operating-temperature ranges.

Varta, for example, touts its lithium/chromium oxide (LiCrOx) batteries as having 70% more energy density than comparable $LiMnO_2$ cells. The company also reports that when it molds coin cells into plastic modules, the self-discharge rate decreases. The increase in life for modules is a result of the extra sealing, which offers additional protection from short-term temperature fluctuations and humidity and also protects against oxidation and contamination.

Even older lithium chemistries are getting updated. For example, Catalyst Research now has lithium iodine batteries that operate over the −55 to +125°C temperature range. Lithium iodine batteries, which are good for as long as 20 years in low-discharge-rate situations, once suited only heart-pacemaker applications because of limited temperature range.

Finally, it's an open secret that all lithium battery makers are working as fast as they can on a rechargeable lithium cell. The holy grail for all these battery designers is an energy density twice that of rechargeable NiCds. Normally, a primary (nonrechargeable) cell has greater capacity than a rechargeable cell of equal size. Moli Energy Ltd was the first company to put a product of this type on the market. The 2.4V cell employs a molybdenum disulfide powder bound to a substrate as a cathode. During discharge, lithium ions move from the lithium anode, through the separator via the electrolyte, and lodge ("intercalate" is the chemist's term) in the porous substrate. During recharge, the lithium ions migrate back and plate themselves onto the lithium anode. The porous substrate solves the problem of getting the metal to plate back onto the anode that has kept lithium (and, incidently, common carbon zinc batteries) from being rechargeable until now.

Unfortunately, lithium batteries pose their own special handling and designing-in problems. Though you can assemble individual cells into a battery yourself, you should realize that the capacity variation among randomly selected cells is normally greater than that recommended for battery assembly. Thus, companies like Tadiran supply categorized batches of cells that you

TABLE 4—LITHIUM SOLID CATHODE CELL CHARACTERISTICS

TYPE OF CELL	OPERATING VOLTAGE (V)	CHARACTERISTICS
Li/MnO_2	3.0	HIGH GRAVIMETRIC AND VOLUMETRIC ENERGY DENSITY; WIDE OPERATING TEMPERATURE RANGE (−20 TO +55°C); PERFORMANCE AT RELATIVELY HIGH DISCHARGE RATES; MINIMAL VOLTAGE DELAY; RELATIVELY LOW COST; AVAILABLE IN COIN AND CYLINDRICAL CELLS
$Li/(CF)_N$	2.6	HIGHEST THEORETICAL GRAVIMETRIC ENERGY DENSITY; LOW TO MODERATE RATE CAPABILITY; WIDE OPERATING TEMPERATURE RANGE (−20 TO +60°C); VOLTAGE DELAY OBSERVED; AVAILABLE IN COIN AND CYLINDRICAL CELLS
Li/CuS	1.7	GOOD VOLUMETRIC ENERGY DENSITY; LIMITED AVAILABILITY—DESIGNED ONLY IN 9V NEDA SIZE 1604; POTENTIAL FOR LOW COST
Li/CuO	1.5	HIGHEST THEORETICAL VOLUMETRIC COULOMBIC CAPACITY (Ahr/L); VOLTAGE COMPATIBLE WITH CONVENTIONAL 1.5V CELLS; LOW TO MODERATE RATE CAPABILITY; OPERATING TEMPERATURE RANGE TO 125 TO 150°C; NO APPARENT VOLTAGE DELAY; AVAILABLE IN CYLINDRICAL CELLS
Li/FeS_X	1.5	DIRECT REPLACEMENT FOR CONVENTIONAL Zn/HgO AND Zn/Ag_2O BUTTON CELLS; LOWER POWER CAPABILITY THAN CONVENTIONAL CELLS, BUT BETTER LOW-TEMPERATURE PERFORMANCE AND STORABILITY; RELATIVELY LOW COST; AVAILABLE IN BUTTON-CELL SIZES
$Li/Bi_2Pb_2O_5$	1.5	REPLACEMENT FOR CONVENTIONAL BUTTON CELLS; OPERATING RANGE FROM −20 TO +50°C; LOW DRAIN, BUT PULSE LOAD CAPABILITY; AVAILABLE IN BUTTON-CELL SIZES
Li/Ag_2CrO_4	3.1	HIGH VOLTAGE; HIGH ENERGY DENSITY; LOW RATE CAPABILITY; HIGH RELIABILITY; USED IN LOW-RATE, LONG-TERM APPLICATIONS; HIGH COST; AVAILABLE IN BUTTON, SMALL RECTANGULAR, AND D-SHAPED CELLS
Li/CrO_X	3.3	HIGH VOLTAGE; HIGH ENERGY DENSITY; LOW RATE CAPABILITY; AVAILABLE IN CYLINDRICAL CELLS
Li/V_2O_5	3.3	HIGH VOLUMETRIC ENERGY DENSITY; 2-STEP DISCHARGE; USED MAINLY IN RESERVE CELLS

(SOURCE: THE HANDBOOK OF BATTERIES AND FUEL CELLS (REF 1))

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CIRCLE NO 110

You shouldn't—and no longer have to—limit your plans for battery backup to just the minimum critical circuitry.

can assemble into batteries without further selection.

If you expect the user of your products to replace batteries, then you must check your battery literature closely. Some batteries are not UL certified for user replacement. For example, because of potential problems from polluting chemicals, possible explosions, and other handling problems, you cannot get UL recognition for thionylchloride lithium batteries.

The reason that thionylchloride (as well as other chemistries) has problems with explosions is its high current capability under short-circuit conditions. High current causes extreme heat, which can lead to cell damage or even explosion. Renata uses a current-limiting technique that limits short-circuit current and makes the company's batteries damage or explosion free. Maxell's $5 to $8 super lithium batteries come in AA, ½AA, and ⅔AA sizes and are UL recognized.

You should also keep in mind that the long shelf life of lithium batteries may not be worth their extra cost if your system will be serviced regularly. In such a case, you might consider using much-cheaper alkaline cells and having the service personnel replace the batteries as part of a regular maintenance routine. After all, many accidents in handling and storage can befall a lithium battery, reducing its shelf life and capacity. You never know, for instance, if a pc board has sat in a boxcar on a siding for a couple of weeks during shipping. High heat or accidental shorting can damage lithium batteries.

Once you've assessed your application's backup battery needs and chosen a battery, you still have to take into account charging circuitry and isolation requirements. The charging circuit associated with your battery can influence your design decisions because different battery types require different charging schemes—some more elaborate than others.

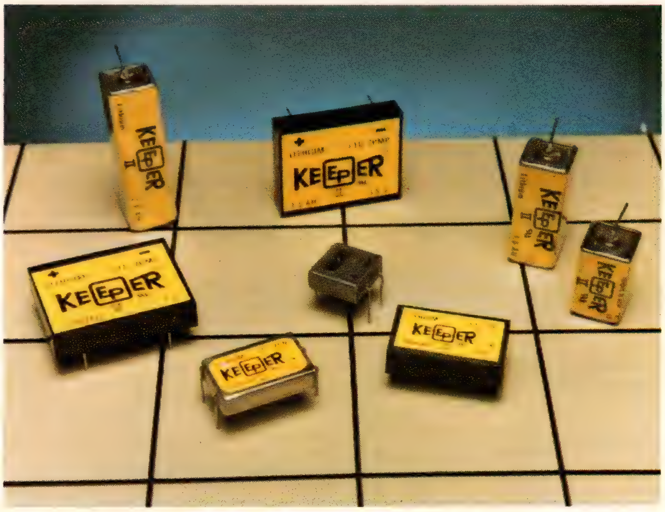
Rechargeable batteries follow the laws of physics: They require that you put more energy back into them than you remove during discharge. Typically this energy ranges from 120 to 140%, based on factors like ambient temperature variations, charger efficiency, and the age of the battery.

Cyclic applications require that the battery recharge overnight: 12 to 14 hours. Normally, this charging requires a current of C/10, where C is the battery-industry standard term for the capacity of a battery. Faster charge rates are available, though. For example, NiCd makers have quick-charge batteries that will recharge in three to five hours and fast-charge batteries that will recharge in one hour. The quick-charge cells will work with a normal charger; the fast-charge units require special battery-temperature sensing and charging-cutoff circuits.

For float applications, you normally charge the battery with a current in the range of C/20 to minimize overcharging and to prolong battery life. Battery manufacturers discourage rates below C/20 because they tend to be inefficient, especially at high temperatures.

Temperature affects charging

Temperature is an important factor in the storage of gelled-electrolyte lead-acid batteries. At 20 to 25°C,



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CIRCLE NO 168

Failure to plan for a drop in capacity at low temperatures will come back to haunt the careless designer.

the gelled cell self-discharges at 2 to 3% per month. However, once a battery has self-discharged to 50% of capacity, you must recharge it. Below the 50% level, the actual rate of self-discharge accelerates.

Of all the methods for recharging batteries, the limited-current/constant-voltage method produces the best results with gelled-electrolyte lead acid batteries. For cyclic-service applications, you should charge gelled cells at 2.4V per cell max with the current limited to a maximum of C/5. You can tell when the battery is charged by monitoring the current it will accept. The trigger point for stopping charging depends on the battery; specific values are available from the manufacturers. You should remove batteries charged at 2.4V/cell from the charger within a few days once they are fully recharged.

For float/standby charging, you should use a voltage of 2.25 to 2.3V per cell. At these levels, the battery can be left on charge for the entire life of the battery. For best battery service, peak-to-peak ripple voltage should not exceed 0.5% of the charging voltage.

NiCds like constant current

According to Sanyo, constant-current charging is the best method for recharging NiCd batteries. You can easily determine the necessary quantity of charge for a given number of cells. However, constant-current chargers are expensive, so most designers employ quasiconstant-current charging. This method involves inserting a resistance between the dc power supply and the cell that produces the near-constant current. You should adjust the value of the resistance so that the charging current is within the limits specified by the battery manufacturer at the end of the charging cycle. Because temperature causes a NiCd cell's voltage to vary considerably, the company doesn't recommend constant-voltage charging. For trickle charging, the battery sees a continuous current that should range from C/20 to C/50.

You should avoid parallel charging. When NiCd batteries are charged in parallel, the difference in charge voltage causes larger current flow into the cell with the lesser charge voltage. Further, the voltage of NiCd types reaches its peak near the end of charging and then decreases after being fully charged, meaning that the charge current could increase and destroy the battery.

Nonrechargeable lithium cells do not perforce require a charging circuit, but you must isolate the battery from the normal power supply and noncritical loads with at least a pair of diodes—and preferably a blocking resistor to protect the battery against reverse current in case of a diode failure. Renata makes molded-plastic modules containing a lithium coin cell and isolation diodes.

Cold temperature or higher discharge rates necessitate a Shottky diode. The diode you choose must have a low leakage current (50 nA or less). Saft recommends the Hewlett-Packard HSCH-1001. With a typical voltage drop of less than 0.3V, this diode is an excellent choice for memory-backup applications.

Estimate backup load carefully

Most IC manufacturers specify their backup current requirements as a maximum (worst-case) value at 85°C. You shouldn't use this value to select the proper size of your batteries without first determining the ambient temperature of your ICs. Saft notes that for every 10°C drop in temperature, the keep-alive current a chip draws will drop by 50%. For instance, a chip using 150 μA at 85°C will use only 2.5 μA at 25°C. The difference in current drawn suggests the use of a less-expensive button cell in place of a cylindrical cell.

Although momentary short circuiting of a lithium battery isn't harmful and has no effect on the capacity of the battery or its electrical performance, you can design in additional long-term short-circuit protection. Tadiran recommends that as an additional safety feature you limit short-circuit current in the event of a serial diode failure by connecting an additional 10-kΩ resistor in series with the diode or by using an additional serial diode. The leakage current of most silicon diodes of a few microamperes doesn't damage lithium batteries. Any general-purpose silicon diode (for example, 1N4148, 1N914, or 1N4002) will work.

In addition, you can employ a pair of jumperable pins on the component side of the pc board to totally disconnect an onboard lithium battery until it's needed. Note that for the case of lithium thionyl chloride batteries, a fresh battery should measure 3.66V. This initial high voltage quickly fades away, but at least your incoming inspection department can tell fresh from stale cells even if your field-service department cannot.

Tadiran further recommends measures to overcome the initial drop in voltage encountered in lithium batteries that have not been under load recently. The passivation layer that forms inside a lithium battery, which gives the lithium battery its long shelf life, has the unfortunate effect of causing a drop in voltage when you first apply a load to the battery.

Text continued on pg 150

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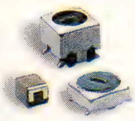

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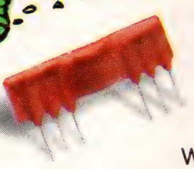

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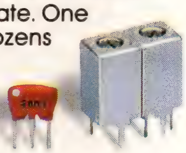

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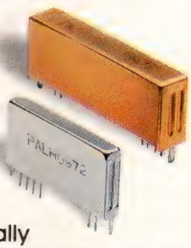

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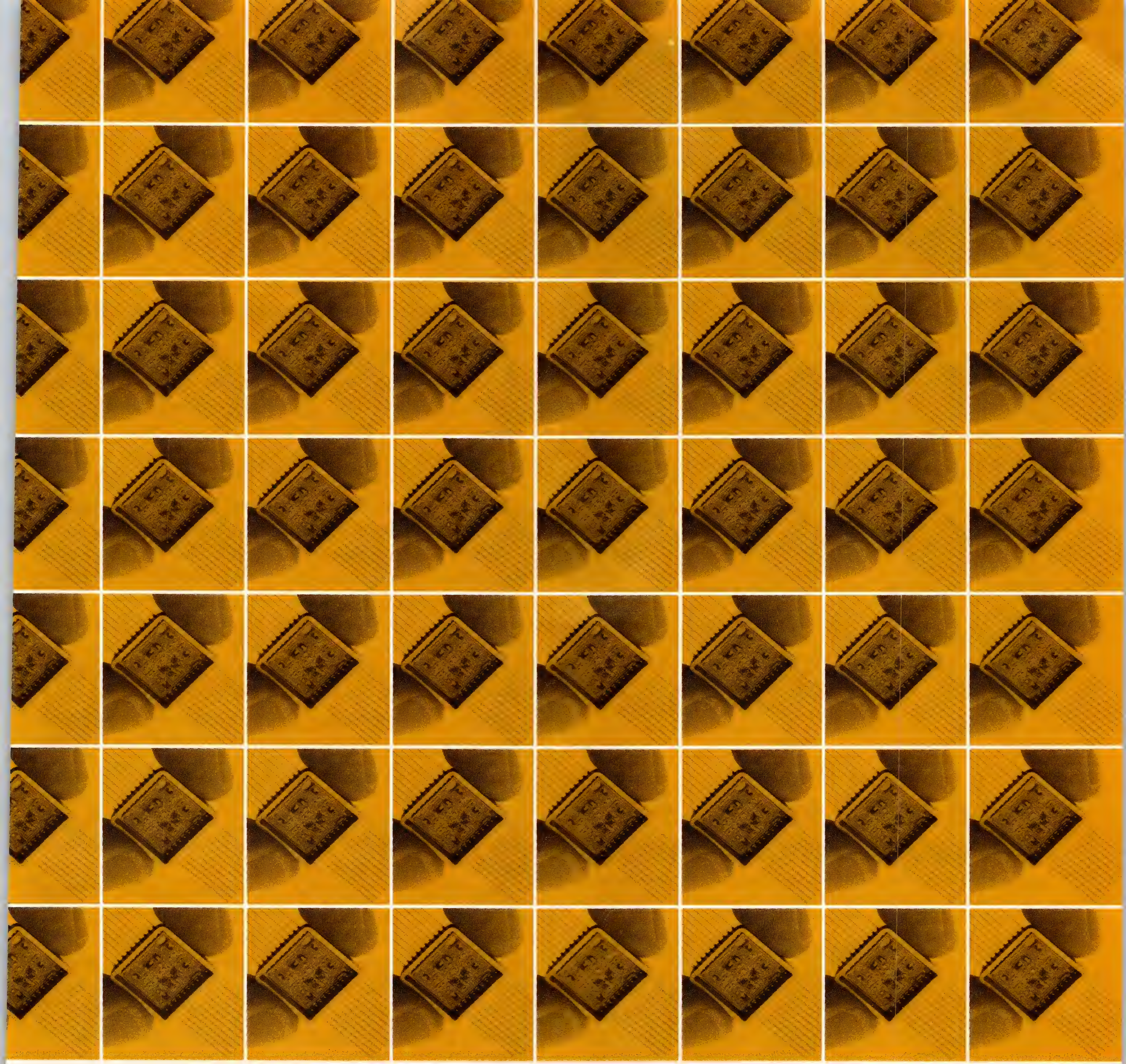

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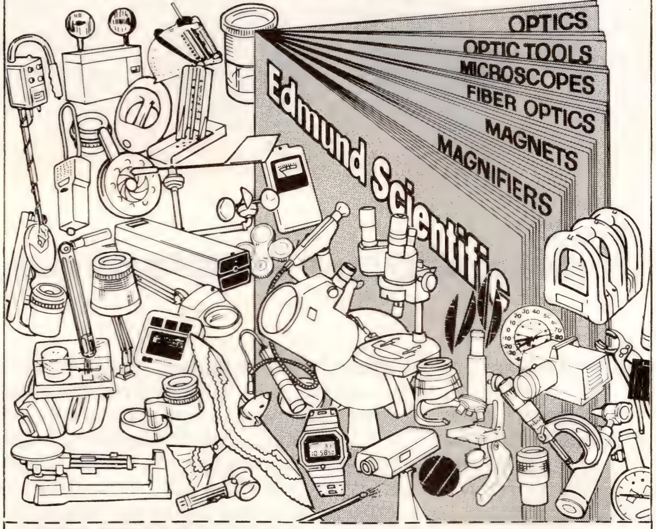

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To overcome this problem, or at least to limit its impact, Tadiran recommends you connect a parallel bleeding resistor to the battery. Continuous leakage current through the cell at the level of 0.02% of the expected peak current will control the thickness and the resistance of the passivation layer and limit the voltage drop at the battery to 3.0V min. You can subtract any standby current drawn by your circuitry from the total bleed current. You can, of course, put a capacitor in parallel with the cell for peak pulses, but the capacitor should be a low-leakage type.

Finally, two caveats are in order. First, your production people should take extra care to make sure that a battery never falls off of a pc board and into molten solder. The result could be a formidable, dangerous, and messy explosion. It should be no surprise that there aren't any surface-mounted batteries available yet.

Second, the chemicals and materials in common battery systems can present hazards. Particularly troublesome is the disposal of old, perhaps partially discharged, units and the handling of fresh ones. Ordinarily, you shouldn't dispose of batteries in sanitary landfills, but instead rely on companies that specialize in battery disposal.

According to Rayovac, you can dispose of small quantities of discharged lithium cells—up to 20—directly in a sanitary landfill. For larger quantities, the company recommends that you first further discharge the cell to convert all remaining lithium metal to an inert substance. You can complete this conversion by putting the cells in graphite for a period of three weeks. The graphite continues the discharge process until all free lithium has been consumed. Depending on cell type, you can pack between 100 and 550 cells per gallon of graphite powder. After the 3-week discharge, you can send the cells to a landfill and re-use the graphite: It is unaffected by the discharging cells. **EDN**

References

1. Linden, David, editor in chief, *The Handbook of Batteries and Fuel Cells*, McGraw-Hill Book Co, NY, NY 1984.

2. Independent Battery Manufacturers Association, *SLIG* [starting, lighting, ignition] *Systems Buyer's Guide*, $8, 100 Larchwood Dr, Largo, FL 33540. Phone (813) 586-1408.

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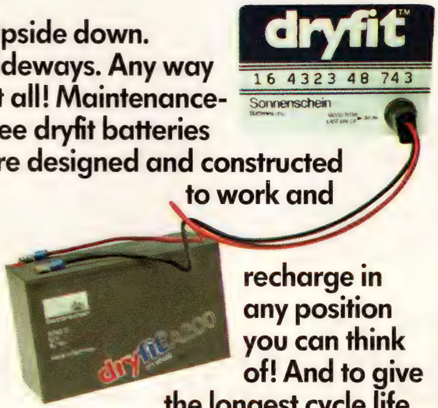

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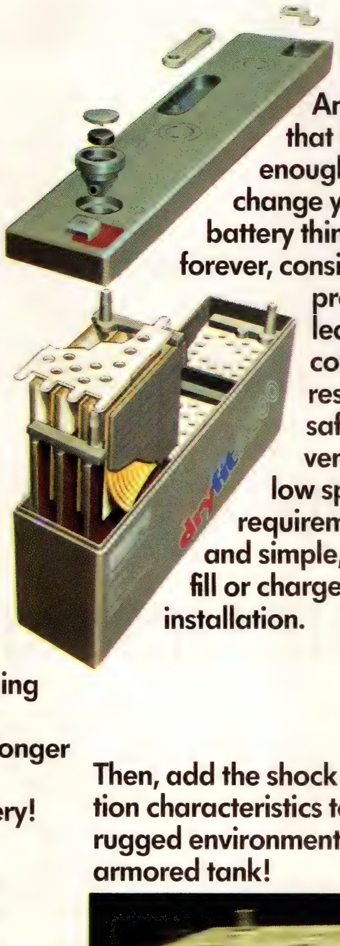

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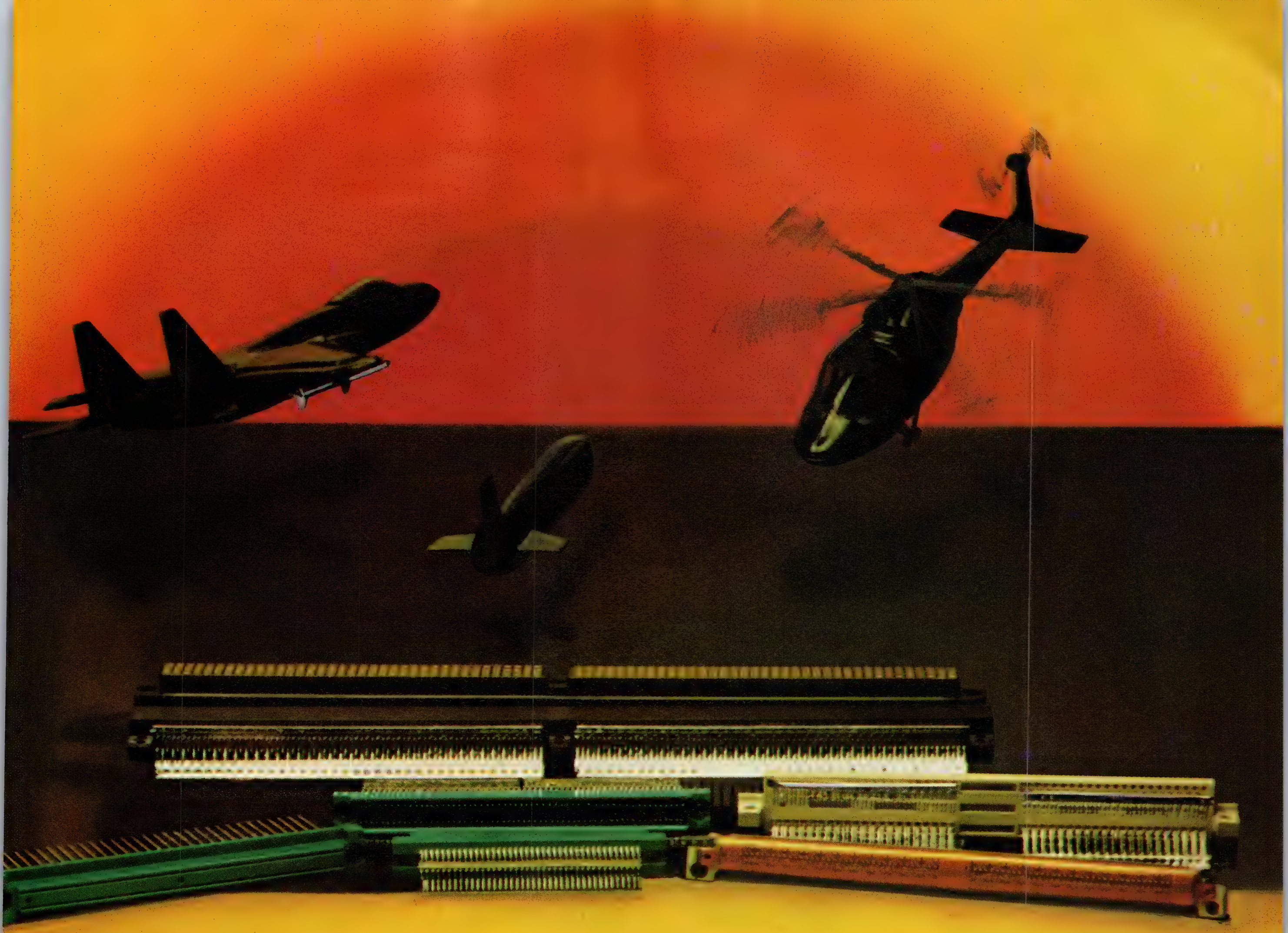

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Single-port MAC speeds 68000 matrix products

A single-port multiplier/accumulator IC overcomes speed constraints placed on system performance by the long multiplication times of μPs. Compared with add-on bit-slice multiplication accelerators, the device offers an easier and more economical solution to multiplication needs in digital-signal-processing applications.

David Fair, *Analog Devices Inc*

In multiplication-intensive applications, the slow multiplication speed of microprocessors often severely constrains system performance. If you want a μP-based system to perform a digital-signal-processing algorithm (for example, digital filtering, graphics transformations, real-time spectrum analysis, or speech synthesis), you're faced with the choice of accepting the μP's poor multiplication throughput or designing an expensive bit-slice multiplication accelerator as an add-on. The ADSP-1110A—a single-port, 16-bit CMOS multiplier/accumulator (MAC) in a 28-pin package—presents another alternative.

The ADSP-1110AJ has a 100-nsec multiplication time with a 50-nsec clock, and the IC's architecture is arranged so that it can load two data inputs concurrently with each multiply/accumulate operation. A higher-grade unit, Model ADSP-1110AK, specs an 85-nsec multiply/accumulate time. You can use low-cost TTL parts to control the ADSP-1110A's operation for bit-slice accelerator performance, at a much lower cost than that of a bit-slice system.

The task of multiplying successive 1×4 matrices (vectors) by a 4×4 matrix—a common operation in applications requiring coordinate transformations—illustrates the acceleration the ADSP-1110A can add to a μP-based system. Performing this arithmetic (four sets of 4-pair, 16-bit multiply/accumulate operations) in a 10-MHz 68000 μP requires at least 1432 cycles or 143 μsec per 1×4 matrix, not including initialization or overflow detection. Even the faster 68010 operating at 10 MHz takes 98 μsec per matrix.

The simple subsystem to be described later uses the MAC IC to perform the same calculation with overflow detection in 1.8 μsec per 1×4 matrix. At 1.8 μsec per vector, the 1110A-based system is 80 times faster than a 68000 and 55 times faster than a 68010. Once initialized, moreover, the subsystem operates independently of its host; the host has control of the system bus and can work on other tasks concurrently. Because of the subsystem's relative host independence, you can easily adapt it to CPUs other than the 68000.

Many applications can benefit from the enhanced multiply/accumulate performance. Digital filtering is a straightforward extension of the multiply/accumulate scheme. (See **Refs 1** and **2** for the arithmetic details of finite-impulse-response, or FIR, and infinite-impulse-

A multiplier/accumulator IC can increase a DSP system's speed to many times that of a system using only the computational facilities of general-purpose µPs.

response, or IIR, filtering, respectively.) A 16-tap FIR filter based on the extension discussed here runs 96 times faster than a 68000 and 69 times faster than a 68010, for example. Other applications you could address by using variations of the scheme include, for instance, fast function generation and fast Fourier transformations.

Operations as matrix multiplications

It's convenient to represent translations, scaling, rotations, and projections of point coordinates as matrix multiplications. Translations are in essence additions or subtractions, but you can represent them in homogeneous-coordinate systems as matrix multiplications. Because homogeneous coordinates allow a uniform mathematical representation for all these key transformations, they're popular in graphics applications.

In homogeneous coordinates, a point in 2-dimensional space is represented by a vector,

$$|xys|,$$

where s is a nonzero scale factor. Its coordinates in 2-dimensional space are (x/s, y/s). Similarly, the 3-dimensional vectors are represented as

$$|xyzs|,$$

where (x/s, y/s, z/s) gives the 3-dimensional coordinates of the point.

Matrix multiplication is nothing more than the repeated multiplication and accumulation of pairs of numbers. In general, the transformation of a vector X with n x_i components, by multiplying it by a matrix T with n^2 t_{ij} components, can be expressed by

$$x'_j = \sum_{j=1}^{n} x_j \cdot t_{ij}.$$

Matrices are typically expressed as arrays of numbers. For a 1×4-by-4×4 matrix multiplication, a standard format would be

$$|x'y'z's'| = |xyzs| \cdot \begin{vmatrix} t_{11} & t_{12} & t_{13} & t_{14} \\ t_{21} & t_{22} & t_{23} & t_{24} \\ t_{31} & t_{32} & t_{33} & t_{34} \\ t_{41} & t_{42} & t_{43} & t_{44} \end{vmatrix}.$$

In this format, y′, for example, would be

$$y' = x \cdot t_{12} + y \cdot t_{22} + z \cdot t_{32} + s \cdot t_{42}.$$

The key transformation matrices for 3-dimensional transformations in a right-handed coordinate system are

$$\text{translation by } (\Delta x, \Delta y, \Delta z)\text{:} \begin{vmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ \Delta x & \Delta y & \Delta z & 1 \end{vmatrix};$$

$$\text{scaling by } (s_x, s_y, s_z)\text{:} \begin{vmatrix} s_x & 0 & 0 & 0 \\ 0 & s_y & 0 & 0 \\ 0 & 0 & s_z & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix};$$

$$\text{rotation of } \Phi \text{ around the x axis:} \begin{vmatrix} 1 & 0 & 0 & 0 \\ 0 & \cos\Phi & \sin\Phi & 0 \\ 0 & -\sin\Phi & \cos\Phi & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix};$$

$$\text{rotation of } \Psi \text{ around the y axis:} \begin{vmatrix} \cos\Psi & 0 & -\sin\Psi & 0 \\ 0 & 1 & 0 & 0 \\ \sin\Psi & 0 & \cos\Psi & 1 \\ 0 & 0 & 0 & 1 \end{vmatrix};$$

and

$$\text{rotation of } \Theta \text{ around the z axis:} \begin{vmatrix} \cos\Theta & \sin\Theta & 0 & 0 \\ -\sin\Theta & \cos\Theta & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix}.$$

Additional matrices can represent the various possible perspective projections or parallel projections of interest. By simply multiplying these 4×4 matrices together in their intended order, you can calculate a single 4×4 transformation matrix, T, that contains all the information necessary to translate, rotate, and project a set of points in 3-dimensional space in one operation.

The computational task reduces to multiplying each point's coordinates, represented by a 4×1 matrix, by T. Because a graphics application might require the transformation by T of thousands of points, the speed at which the system can perform this matrix multiplication can have a great impact on system performance. (Two-dimensional transformations are very similar to 3-dimensional ones; for purposes of illustration, this article focuses on 3-dimensional transformations.)

Single-chip, fixed-point multipliers like the ADSP-1110A can lower system cost and improve throughput. But the benefits offered by a fixed-point multiplier depend in a critical way on the IC's interface to the host system. Three acceleration-device/µP interface methods are distinguishable (in order of increasing performance and complexity): You can realize the interface through standard memory (or I/O) mapping, through block-transfer memory mapping, or by controlling the acceleration device independently and allowing it independent access to data memory.

In a standard memory-mapping implementation, the acceleration device only has to run fast enough to have a product ready when the host reads back the result. No advantage accrues from using multipliers that are faster than the relevant data-transfer rates. Accelerating multiplications with standard memory mapping is not worth the trouble. Fixed-rate word-multiplication times for the latest generation of µPs have been reduced to roughly the time required for three data-move operations.

Motorola's MC68010, the 16-bit data-path successor to the MC68000, can do a signed word multiplication in 42 cycles rather than the 70 cycles of its predecessor. Three word-length move operations require 36 cycles—in the best case—while tying up the system bus, which is why standard memory mapping is hardly worthwhile. Standard memory mapping does, however, provide some limited benefits for multiplication/accumulation operations if the number of product terms is large enough. That's because a multiply/accumulate operation without reading back requires only two word-move operations (24 cycles in the best case), allowing an acceleration effort that asymptotically approaches approximately 40% as the number of pairs of multiplicands in the summation increases.

Block-transfer mapping

When an application like matrix multiplication or digital filtering requires a series of accumulated products, it's possible to move blocks of data down the system bus at higher rates to improve throughput. As in standard memory mapping, the acceleration device sits on the host's data bus. The difference is that in block-transfer memory mapping, multiple data words move in back-to-back bus cycles.

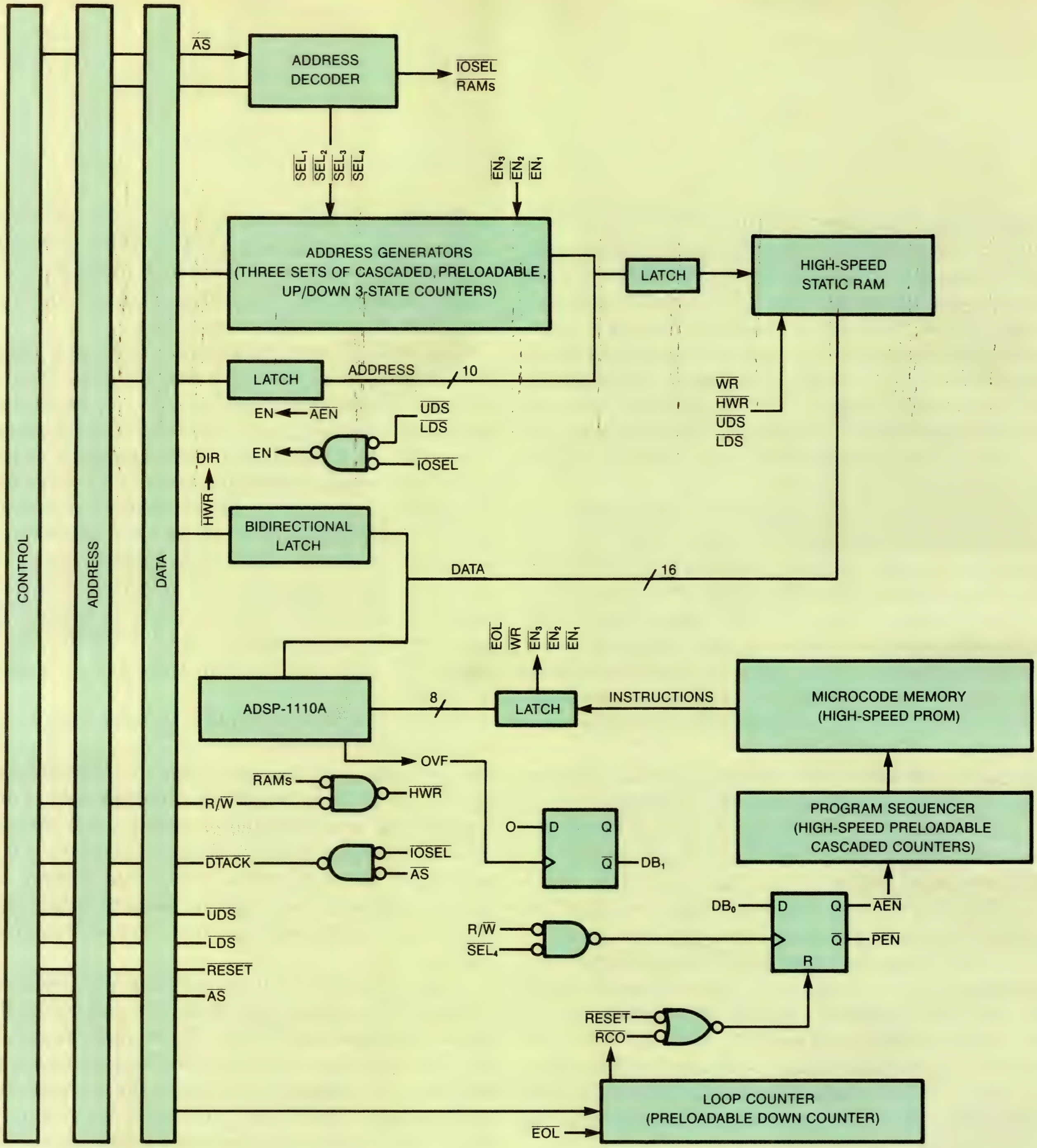
The devices in the 68000 family accommodate a multiple-move instruction, MOVEM, that moves as many as 16 consecutive data words (corresponding to the µP's eight data registers and eight address registers) at the maximum bus transfer rate—800 nsec for each pair of words with a 10-MHz 68000 or 68010. In practice, you would move fewer than 16 words, because indirect addressing—the fastest mode—requires the use of one or more address registers.

With MOVEM, you could move as many as eight pairs of multiplicands on the data bus and read them into your acceleration device as they pass by. At the cost of additional complexity, you could add a direct-memory-access (DMA) controller for data transfers of larger blocks. Multiply/accumulate rates of 800 nsec would significantly accelerate a µP's operation, especially as the number of product terms in each summation increases. Calculation of a 4-pair multiply/accumulate operation could take place in 52 cycles, a sevenfold improvement over the 10-MHz 68000 (in the best case) and a fivefold improvement over the 68010. The only type of IC that can maintain that pace is a parallel multiplier.

The main problem with block-transfer memory mapping is that it requires the interleaving of pairs of multiplicands in consecutive locations. This constraint can result in large overhead requirements in many applications, rendering the preceding performance improvement largely theoretical. A second problem is that controlling the acceleration device can become much more complicated than simple memory mapping, because the system requires more complex control sequences.

A natural solution to the interleaving problem for operations like matrix multiplication and digital filtering is to put one set of terms (for example, transformation-matrix terms or filter coefficients) into a local memory. By multiplexing between the system bus and local memory, this solution also allows you to double the rate of data input to the acceleration device (to 400 nsec per input pair). Unfortunately, this method increases still further the complexity of the addressing and control problems. Virtually all the advantages of a direct data-bus interface between the host and the acceleration device are lost by the time you add memory multiplexing to block-transfer memory mapping.

In addition to these disadvantages, block-transfer memory mapping with or without local memory multiplexing takes advantage of only a fraction of the raw computation speed a device like the ADSP-1110A offers. The third interface approach **(Fig 1)**, which is in effect an implementation of an acceleration subsystem, takes full advantage of the ADSP-1110A's multiply/accumulate speed. In an acceleration subsystem with



MNEMONIC	DESCRIPTION
PEN	ENABLE MMA (ACTIVE LOW)
AEN	ENABLE HOST ACCESS TO RAM (ACTIVE LOW)
IOSEL	ADDRESS ON SYSTEM BUS IS IN MMA'S ADDRESS SPACE (ACTIVE LOW)
RAMs	ADDRESS ON SYSTEM BUS IS IN MMA'S RAM SPACE (ACTIVE LOW)
HWR	HOST WRITE TO MMA'S RAM (ACTIVE LOW)
SEL_x	INITIALIZATION CONTROLS (ACTIVE LOW)
EN_x	ENABLE ADDRESS-GENERATOR X (ACTIVE LOW)
EOL	END-OF-LOOP (ACTIVE LOW)
WR	WRITE FROM ADSP-1110A TO RAM (ACTIVE LOW)
OVF	ADSP-1110A OVERFLOW
DB_x	MMA'S DATA-BUS BIT X

*Fig 1—**The matrix-multiplication accelerator (MMA)** brings microcode performance to a μP-based system. It uses standard TTL circuits for address generation and microcode sequencing. The system uses fast static RAM that's shared by the MMA and the 68000 μP. This subsystem is much faster than those based on memory mapping.*

It's convenient to represent translations, scaling, rotations, and projections of point coordinates as matrix multiplications.

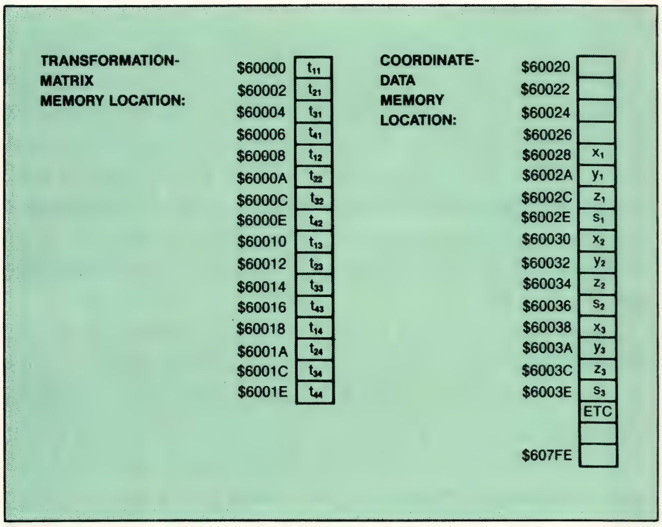


Fig 2—A map of the shared static-RAM memory space *shows that the shared-RAM space lies between hexadecimal addresses $60000 and $607FF. The MMA finds the transformation-matrix's 16 words in the RAM's low-order portion; coordinate-data vectors can start anywhere thereafter in the shared memory.*

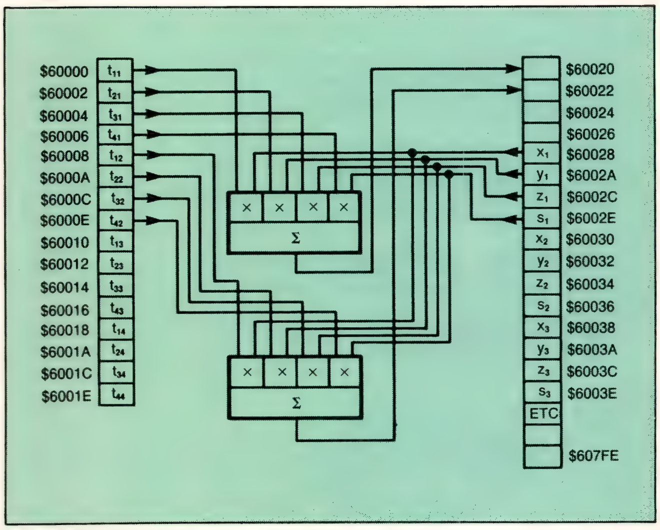


Fig 3—Illustrating the matrix-multiplication process, *this diagram shows the flow of operations performed on the variables stored in the shared-memory portion of the static RAM. The complete matrix multiplication consists of four sets of 4-pair multiplication/accumulation operations.*

independent control and independent access to high-speed data memory, the IC can run at speeds far faster than the data-transmission rates of a 68000-family device. Though more complex than memory mapping, the subsystem, called here a matrix-multiplication accelerator (MMA), can use standard, inexpensive TTL parts. You could use programmable logic arrays or gate arrays to simplify the design even further.

The MMA uses standard TTL binary up/down counters for address generation and microprogram sequencing. The design brings microcode performance to a µP-based system at low cost. The MMA, built around an ADSP-1110A and high-speed system memory, requires about 30 additional SSI and MSI parts that cost approximately $50 in quantities of 100. The system takes about 30 in^2 of board space. You can build accelerators for such algorithms as digital filtering with similar part counts and costs.

Memory organization uses static RAM

The 68000 and the MMA share 1024 words (easily expandable) of 25-nsec static RAM (for example, Cypress's CMOS CY7C149) in the 68000's address space. In the illustration used here, the shared system memory is mapped between hexadecimal addresses $60000 and $607FF. The MMA expects to find the 16 words representing the transformation matrix in the 16 low-order words of the shared RAM **(Fig 2)**. Coordinate data vectors can start anywhere in the shared RAM thereafter.

Assume all data is in 2's-complement format, although it's only necessary to change the microcode pattern in PROM to handle unsigned-magnitude or mixed-mode calculations. Holding the ADSP-1110A's instruction bit 3 high indicates a 2's-complement X input for arithmetic instructions; a low state indicates an unsigned-magnitude X input. Input-data format selection for the Y input, controlled similarly by instruction bit 4, is totally independent of X-input selection. The memory-mapped initialization of the MMA uses the four word addresses $60800 through $60807, which are just past the shared RAM space.

The MMA can write the updated coordinate-data vectors anywhere in the shared memory. This flexibility comes about by using independent, preloadable counters for generating data-read and data-write addresses. To minimize both memory requirements and data-setup overhead, the MMA can increment while writing results to the previous vector locations, or it can decrement from the top of the data space while writing results to the next-higher vector address.

To see how a matrix multiplication works, consider the case in which you write results to the previous vector location. To read data into the ADSP-1110A, one counter must point to t_{11} ($60000), a second to x_1 ($60028 in this example). Both these counters increment during

The benefits offered by a fixed-point multiplier depend in a critical way on the IC's interface to the host system.

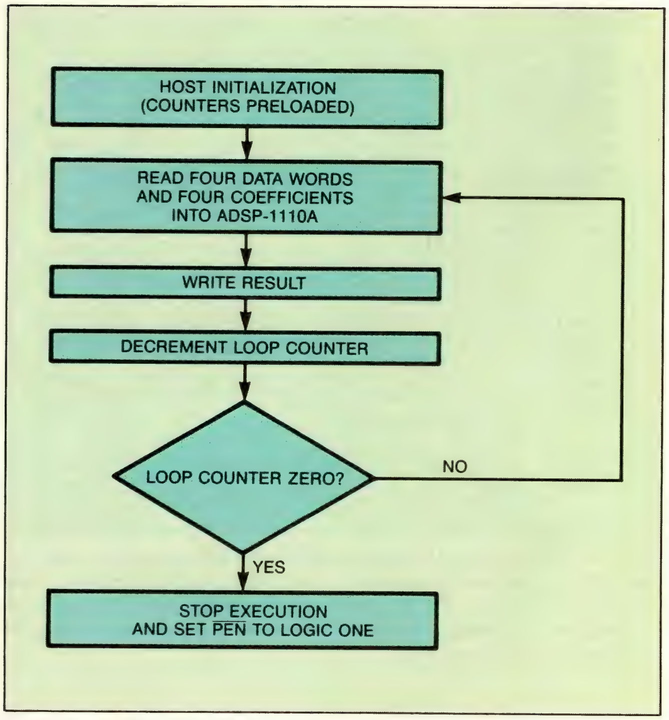

HOST INITIALIZATION (COUNTERS PRELOADED)
READ FOUR DATA WORDS AND FOUR COEFFICIENTS INTO ADSP-1110A
WRITE RESULT
DECREMENT LOOP COUNTER
LOOP COUNTER ZERO?
NO
YES
STOP EXECUTION AND SET $\overline{\text{PEN}}$ TO LOGIC ONE

***Fig 4—Program sequencing for the MMA** follows this flowchart. Microcode that controls the ADSP-1110A and the address generators comes from a PROM in the MMA's control section. A cascaded pair of 4-bit up counters serves as the program's sequencer.*

a data-read operation until they generate four pairs of addresses. A third counter indicates where to write the results.

The MMA writes its first 4-pair multiply/accumulate result, x'_1, to the first position of the previous data vector ($60020), as shown in **Fig 3.** Because results are written to the previous 4-word vector, the current read data remains stable until its transformation is complete. For the 4-pair multiply/accumulate that generates y'_1, the transformation-matrix address counter continues to the fifth term, t_{12} (at $60008). The data-read address counter, however, must again generate the addresses where x_1, y_1, z_1, and s_1 are located ($60028 through $6002E). Before y'_1 is written back to RAM, the data-write address counter must increment to the next word address ($60022).

The complete matrix multiplication consists of four sets of these 4-pair multiplication/accumulation operations. The transformation-matrix address counter increments steadily through the 16 terms. The data-read address counter generates addresses that cycle through the four input-data words four times. The data-write address counter increments four times—once after each result is written.

For the next matrix multiplication, the transformation-matrix address counter must return to t_{11}'s address. The data-read counter must move on to the next 4-word vector, where it will cycle through all four words four times. The data-write counter simply increments to the next sequential word. Consequently, the result of updating the second source-data vector is written in the locations that had contained the first source-data vector, and so on.

If you want results to be written at address locations higher than the addresses of the source-data vectors, you can instruct the MMA to start the matrix multiplication with t_{44} and the last word of your last data vector and then decrement, rather than increment, all counters. Because it makes no difference when accumulating four pairs of products whether you start with the first or the last pair, the same microcode program for the ADSP-1110A works in either direction. The MMA's flexibility in being able to write below the block of source data and increment, or write above the source data and decrement, can save RAM and greatly reduce memory-management overhead.

Program sequencing for the MMA follows the flowchart shown in **Fig 4.** Microcode that controls both the ADSP-1110A and the address generators comes from PROM in the control section of the MMA. A cascaded pair of 4-bit up counters (F163s) serves as the program sequencer. A microcode bit (EOL) indicates an end-of-loop condition. That signal causes the program sequencer to reset to zero for the next matrix multiplication. These counters are the only ones in the MMA that must count and reset at a 20-MHz rate.

An 8-bit down counter (an AS867) in the control section serves as the loop counter and is preloaded by the 68000 with the number of vectors to be updated. After each matrix multiplication, the counter decrements by 1. When it reaches 0, it generates a signal ($\overline{\text{RCO}}$) that stops the MMA. $\overline{\text{AEN}}$ goes low, allowing the host access to the shared RAM, and its complement ($\overline{\text{PEN}}$) goes high. If the host polls data bit 0 (DB_0), it will find it equal to $\overline{\text{PEN}}$ (a logic one), indicating that the MMA is no longer busy. If the ADSP-1110A had overflowed during any multiply/accumulate operation, the OVF line's going high would have set a flip-flop, so data bit 1 (DB_1) would be a logic one. Microcode for the MMA, stored in PROM, is shown in **Table 1.**

The address generators consist of three sets of ALS569 cascaded up/down, 4-bit, 3-state counters. Two bits of microcode **(Table 2)** control the address genera-

TABLE 1—
PROM MICROCODE FOR MMA

PROM BIT	MEANING
0	ADSP-1110A PIN 10
1	ADSP-1110A PIN 11
2	ADSP-1110A PIN 12
3	ADSP-1110A PIN 13
4	ADSP-1110A PIN 14
5	ADSP-1110A PIN 15
6	ADSP-1110A PIN RND14/SLE
7	ADSP-1110A PIN RND15
8	ADDRESS-ENABLE BIT ZERO (AEB_0)
9	ADDRESS-ENABLE BIT ONE (AEB_1)
10	$\overline{\text{WR}}$—WRITE DATA TO RAM (ACTIVE LOW)
11	$\overline{\text{EOL}}$—END-OF-LOOP (ACTIVE LOW)

TABLE 2—
ADDRESS-GENERATOR MICROCODE

MICROCODE		ACTION
AEB_1	AEB_0	
0	0	NULL
0	1	GENERATE ADDRESS FOR TRANSFORMATION-MATRIX COEFFICIENT AND INCREMENT/DECREMENT COUNTER
1	0	GENERATE ADDRESS FOR DATA READ AND INCREMENT/DECREMENT COUNTER
1	1	GENERATE ADDRESS FOR DATA WRITE AND INCREMENT/DECREMENT COUNTER

tors. Each counter's active-low enable control does double duty by incrementing or decrementing the selected counter as it returns high. Because the same set never increments twice in succeeding clock cycles, the counters will never be incremented and enabled in the same 50-nsec clock cycle; 10-MHz counters are therefore adequate.

The transformation-matrix address generator and the data-write address generator change in a monotonic manner by increments or decrements of 1. Because the data-read vector is cycled through four times to produce an updated destination vector, the data-read address generator uses only the two least-significant bits of the lowest-order counter for address generation; the third and fourth counter output pins are ignored (no connection), and address bit 3 comes from the fifth counter output pin.

The 50-nsec cycle time makes demands on memory and TTL components. As a consequence, all flows of microcode, addresses, and data are latched with the MMA's 20-MHz clock. Because address generation requires a 50-nsec cycle and reading or writing to RAM takes another cycle, it's necessary to latch microcode

Microprocessor acceleration

The primary design goals for general-purpose μPs are application flexibility and ease of system implementation. Computational speed is only of secondary concern. Many applications requiring the cited virtues, however, also need high-speed number-crunching capabilities.

Several approaches to enhancing the performance of μP-based systems through arithmetic acceleration are available to the systems designer. Some of the more popular solutions involve add-on array-processor units, coprocessor ICs, programmable 1-chip digital signal processors, and DSP multiplier/accumulators in microcoded or bit-slice environments. The ADSP-1110A offers bit-slice acceleration for the price of a single-chip DSP processor.

Array processors can dramatically improve system performance, but these products are generally too expensive for μP-based systems. They can cost more than the anticipated selling price of the system under design. Furthermore, they can be difficult to program and to interface to their hosts.

Coprocessor ICs provide a popular way of accelerating μP algorithms requiring floating-point arithmetic and computation of such high-level functions as square roots, sine values, and logarithms. The coprocessors accomplish in hardware what would otherwise require cumbersome and slow software routines.

Coprocessors don't accelerate basic fixed-point multiplications, however. An Intel 8087 (or 80287) does nothing to make an 8086 or 8088 (or 80186 or 80286) perform a basic 16-bit fixed-point multiplication any faster. Nor does Motorola's 68881 coprocessor for the 68000 family accelerate the μPs' basic multiplication speeds.

If fixed-point multiplication speed is the bottleneck in your application, then coprocessors don't help. Vector transformations for graphics and real-time digital filters are examples of applications in which coprocessors typically add little or nothing to throughput.

TABLE 3—READ AND WRITE RAM CYCLES

READ CYCLE (150 nSEC)	**WRITE CYCLE** (150 nSEC)
1. GENERATE AND LATCH ADDRESS MICROCODE	1. SAME AS READ CYCLE
2. GENERATE AND LATCH ADDRESS; GENERATE AND LATCH 1110A MICROCODE	2. SAME AS READ CYCLE
3. READ RAM AND X OR Y=BUS	3. BUS=MS AND WRITE RAM

for the address generators one cycle before the ADSP-1110A clocks in a read instruction (either X=BUS or Y=BUS). The WR active-low microcode bit drives the RAM's write controls. (**Table 3** gives details of the read and write sequences; **Table 4** gives the complete microcode program for the MMA.)

The host must specify the source and destination starting-word addresses (the 10 high-order bits of their 11-bit-byte address), the number of 4-word data vectors (as many as 255), and whether to increment (logic one) or decrement (logic zero) when addressing the data vectors and transformation coefficients. This information is contained in the four words the 68000 moves to the addresses just beyond the shared memory space ($60800 through $60807), as shown in **Fig 5.**

The MMA decodes the host's MOVEM instruction to these addresses and generates active-low signals for the initialization (**Fig 6**): $\overline{SEL_1}$ from $60806, $\overline{SEL_2}$ from $60804, $\overline{SEL_3}$ from $60802, and $\overline{SEL_4}$ from $60800. With a 68000, the MOVEM instruction is the fastest way (at 28 cycles) to write from registers to memory. MOVEM only works in the *predecrement* mode for this type of move, so the first write event is to $60806. When $\overline{SEL_1}$ goes high, the loop counter in the control section of the MMA is preloaded with the number of data vectors to be updated.

Bits indicating whether each of the three sets of address counters is to increment or decrement are also latched and made available to these counters thereafter. When $\overline{SEL_2}$ goes high, the starting address for data-read operations is preloaded to counters in the MMA's address generator. When $\overline{SEL_3}$ goes high, the starting address for data-write operations is preloaded to another set of counters. When $\overline{SEL_4}$ goes low, it resets the overflow flag (DB_1) in the status register to a logic zero. Execution begins when $\overline{SEL_4}$ goes high while DB_0 on the system bus is at a logic one: $\overline{PEN}$ goes low, its complement ($\overline{AEN}$) goes high, and the host is cut off from the local address and data buses.

During execution, a read event from $60000 will find DB_0 on the system bus at a logic zero, a state that means "busy." The host can then poll this status register to see if the MMA has finished its operation. The host can shut down the MMA and regain control of shared RAM at any time by writing a logic zero on DB_0 to the status register. DB_1 in the status register will assume a logic one if the ADSP-1110A overflows in any multiply/accumulate operation.

If you so choose, you can easily modify this interface so that it sends interrupt signals (that differ in the case of overflow) to the 68000 host at the end of execution. For short operations, you could modify the system to refrain from asserting data acknowledge ($\overline{DTACK}$) until the operation is complete, thereby avoiding interrupt overhead. Another possible (and easy) enhancement would be to latch the output of the loop counter upon overflow of the ADSP-1110A and make the counter's contents available to the host for error tracing and recovery. Because the MMA operates independently of its host, adapting this subsystem's interface to hosts

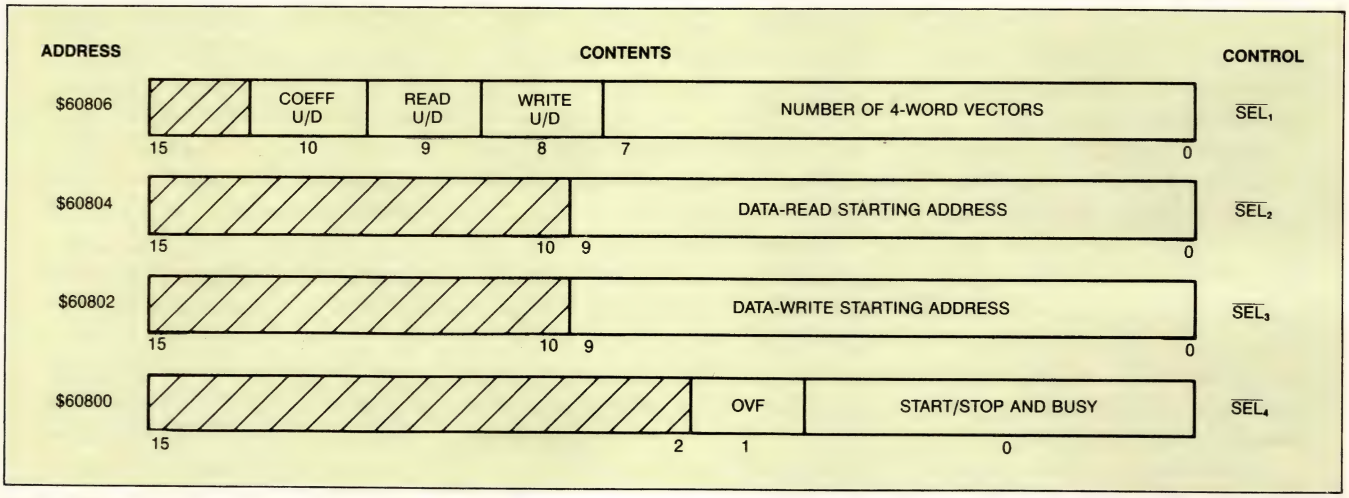


Fig 5—The initialization memory map for the MMA *shows that source and destination starting-word addresses, as well as information about the number of data vectors, increment/decrement instructions, and transformation coefficients, are contained in the four words the 68000 moves to the addresses just beyond the shared-memory space.*

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PM-7541A *Multiplying 12-Bit*	*1/2*		*1*	
PM-7545 *Latched 12-Bit*	*1/2*		*2*	
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The matrix-multiplication accelerator can write updated coordinate vectors anywhere in the shared memory.

TABLE 4—MATRIX-MULTIPLICATION ACCELERATOR MICROCODE

PROM		ACTION	ADDRESS GENERATOR					ADDRESS OUTPUT FROM LATCH	CONTENTS OF MR REGISTER
ADDRESS	CYCLE		1110A MICROCODE	RND	INPUT	WR	EOL		
0		NOP	000000	00	00	1	1	???	GARBAGE
1		GENERATE x ADDRESS	000000	00	01	1	1	???	
2		READ x/X = BUS	001000	00	10	1	1	01-x	
3		READ t_{11}/Y = BUS; Xtc•Ytc; CKMR	111000	00	01	1	1	10-t	
4	1	BEGIN LOOP: READ y/X = BUS	001000	00	10	1	1	01-y	GARBAGE
5	2	READ t_{21}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	00	01	1	1	10-t	
6	3	READ z/X = BUS	001000	00	10	1	1	01-z	$x \bullet t_{11}$
7	4	READ t_{31}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	00	01	1	1	10-t	
8	5	READ s/X = BUS	001000	00	10	1	1	01-s	$x \bullet t_{11} + y \bullet t_{21}$
9	6	READ t_{41}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	01	01	1	1	10-t	
10	7	READ x/X = BUS	001000	00	10	1	1	01-x	3 PAIRS
11	8	READ t_{12}/Y = BUS; Xtc•Ytc; CKMR	111000	00	11	1	1	10-t	
12	9	BUS = MS(sl)/WRITE x′	011000	00	01	0	1	11-x′	4 PAIRS
13	10	READ y/X = BUS	001000	00	10	1	1	01-y	
14	11	READ t_{22}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	00	01	1	1	10-t	
15	12	READ z/X = BUS	001000	00	10	1	1	01-z	1 PAIR
16	13	READ t_{32}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	00	01	1	1	10-t	
17	14	READ s/X = BUS	001000	00	10	1	1	01-s	2 PAIRS
18	15	READ t_{42}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	01	01	1	1	10-t	
19	16	READ x/X = BUS	001000	00	10	1	1	01-x	3 PAIRS
20	17	READ t_{13}/Y = BUS; Xtc•Ytc; CKMR	111000	00	11	1	1	10-t	
21	18	BUS = MS(sl)/WRITE y′	011000	00	01	0	1	11-y	4 PAIRS
22	19	READ y/X = BUS	001000	00	10	1	1	01-y	
23	20	READ t_{23}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	00	01	1	1	10-t	
24	21	READ z/X = BUS	001000	00	10	1	1	01-z	1 PAIR
25	22	READ t_{33}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	00	01	1	1	10-t	
26	23	READ s/X = BUS	001000	00	10	1	1	01-s	2 PAIRS
27	24	READ t_{43}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	01	01	1	1	10-t	
28	25	READ x/X = BUS	001000	00	10	1	1	01-x	3 PAIRS
29	26	READ t_{14}/Y = BUS; Xtc•Ytc; CKMR	111000	00	11	1	1	10-t	
30	27	BUS = MS(sl)/WRITE z′	011000	00	01	0	1	11-z′	4 PAIRS
31	28	READ y/X = BUS	001000	00	10	1	1	01-y	
32	29	READ t_{24}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	00	01	1	1	10-t	
33	30	READ z/X = BUS	001000	00	10	1	1	01-x	1 PAIR
34	31	READ t_{34}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	00	01	1	1	10-t	
35	32	READ s/X = BUS	001000	00	10	1	1	01-s	2 PAIRS
36	33	READ t_{44}/Y = BUS; Xtc•Ytc + MR; CKMR	111010	01	01	1	1	10-t	
37	34	READ x/X = BUS	001000	00	10	1	1	01-x	3 PAIRS
38	35	READ t_{11}/Y = BUS; Xtc•Ytc; CKMR	111000	00	11	1	0	10-t	
39	36	BUS = MS(sl)/WRITE s′/GENERATE y ADDRESS	011000	00	10	0	1	11-s′	4 PAIRS

other than the 68000 family is a straightforward task.

The ADSP-1110A multiplier/accumulator is much faster than such available single-chip DSP processors as the TMS320. The 16-bit TMS32010 operates at 10 MHz and has 400-nsec multiply/accumulate time. Unlike the ADSP-1110A, the TMS320 cannot transfer data on or off chip while performing its multiply/accumulate operation. Configured as described here, the 1110A is 5.7 times faster than the 32010 for each 1×4-vector output, even if you assume the 32010 has all coefficient and input data on chip.

Moreover, the 32010 is limited to 144 words (a transformation matrix and 30 coordinate vectors) in its on-chip data RAM. So, in an actual implementation involving many points, the performance difference approaches a factor of 6.7; an extra 200 nsec is required for each word-length data input. This comparison assumes that the 32010 is configured in an independent acceleration subsystem with support hardware similar to that described here for the ADSP-1110A. Otherwise, it encounters the bottlenecks of memory mapping and can't run any faster than the 68000 bus allows. What's more, the 32010 can't directly address off-chip data RAM with 200-nsec reads, so it still needs address generators to run at its fastest rate.

A digital finite-impulse-response filter, like a matrix multiplication, requires the calculation of a sum of products. The fundamental convolution equation for FIR filters is

$$y_i = \sum_{j=0}^{n-1} h_j \cdot x_{i-j}$$

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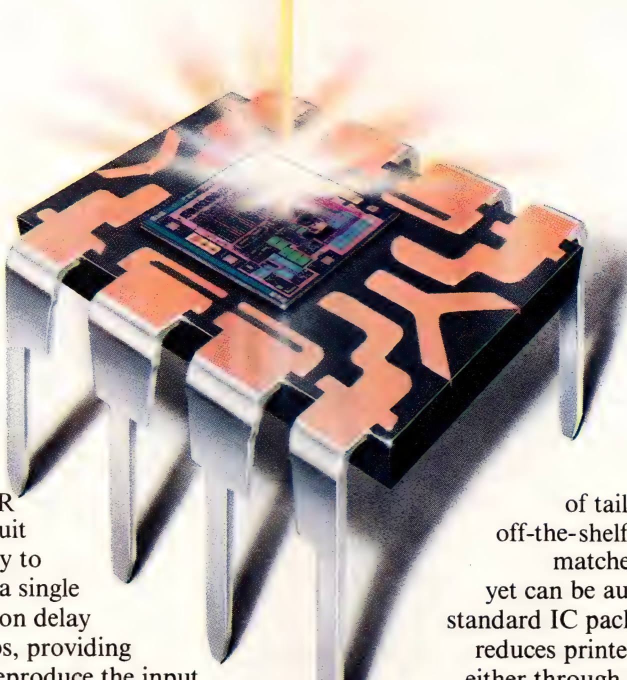

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Because the MMA operates independently of its host, adapting the subsystem's interface to hosts other than the 68000 family is a straightforward task.

where {h} represents the filter-coefficient vector array and {x} is the input-data vector array, which typically represents successive time samples from an A/D converter. The {y} output-data array is a filtered version of the {x} array.

The number n in the equation is the number of taps in the filter. For an FIR filter, the number of taps is generally much greater than four. Therefore, an implementation using the ADSP-1110A for FIR-filter calculations will incur an even smaller throughput penalty (arising from the single I/O port) than does the matrix-multiplication accelerator. The smaller penalty accrues from the fact that outputs from the accumulator are relatively infrequent (as compared with multiply/accumulate operations) in FIR filters.

FIR filter is easy to implement

In many respects, the algorithm for FIR filtering is easier to understand and implement than the one for matrix multiplication. All counters increment or decrement in a monotonic fashion, so the addressing scheme for data-read address generation is simpler than that of the MMA. The data-read address generator's pins connect to the address bus in exactly the same way as those of the data-write address generator.

In addition, it's possible to overwrite the first (oldest) data point as soon as all data-read operations within the FIR filter's window are complete; the read data doesn't have to remain stable for successive multiply/accumulate operations, as it must in the matrix-multiplication algorithm. The easiest way to implement an FIR filter with this hardware is to do exactly that—overwrite the oldest data point with each multiply/accumulate operation.

The filter coefficients can reside in RAM in either normal or reversed order, setting the up/down-counting options as appropriate, so that the first product is $h_{n-1} \cdot x_{j-(n-1)}$. For filters with more than 16 taps, it's a simple task to cascade the coefficient address generator to whatever address space is required. You can use the end-of-loop microcode bit to reset these counters. You should initialize both the data-read and data-write address generators to the address of the first (or oldest) data point.

The FIR-filter accelerator alternately reads data and coefficients into the ADSP-1110A, incrementing or decrementing in a monotonic manner until it reaches the ends of the coefficient and data buffers. At the end of the loop, the results of the multiply/accumulate operation are written to the location of the first data point. The data-write address generator postdecrements or postincrements; it's necessary to reset the data-read generator by preloading this decremented or incremented address.

For this reset function, the output-enable and count-enable lines on the data-write address generator must be separate and independent. The reset causes the data-read address generator to start with the *second* of

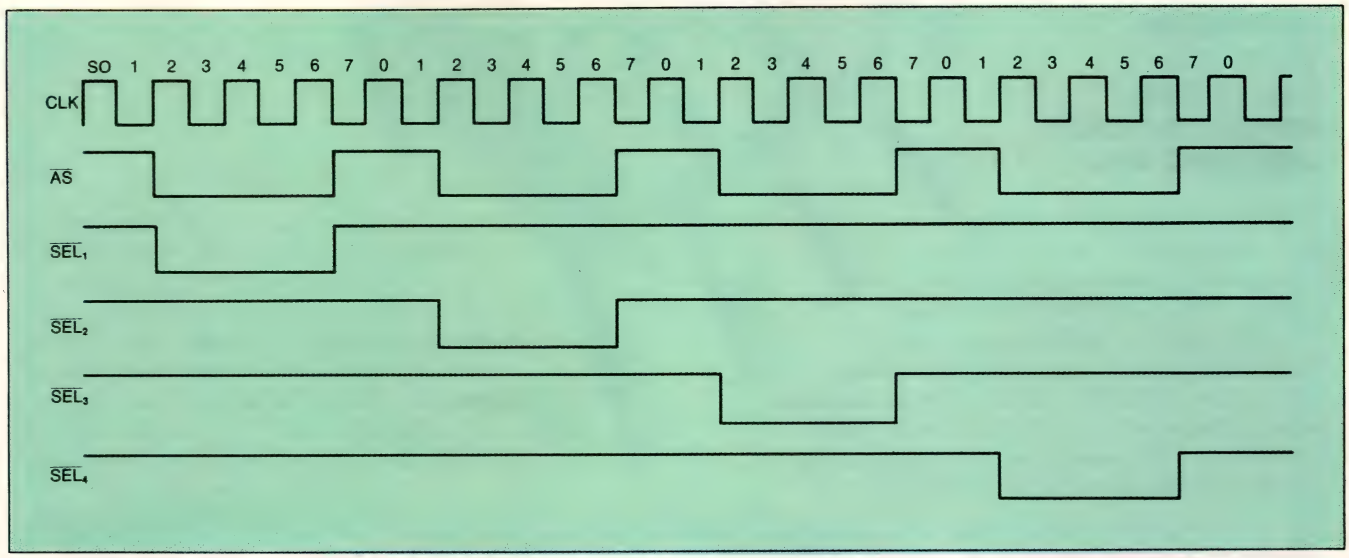
SO 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0
CLK
AS
SEL1
SEL2
SEL3
SEL4

***Fig 6—The 68000 write cycle and MMA initialization controls** are the active-low $\overline{SEL}$ signals. The MMA decodes the host µP's MOVEM instruction to the addresses shown in **Fig 5,** and it generates the active-low signals for the initialization. A MOVEM instruction is the fastest way (with a 68000) to write from registers to memory.*

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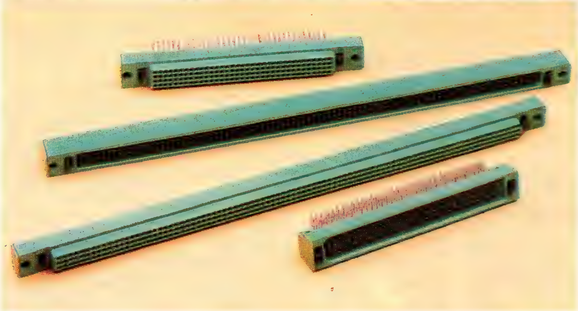

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the original data points on the second pass, effectively shifting the FIR-filter window over by one word.

The microcode program for the FIR-filter accelerator is simply a modification of the MMA's microcode program shown in **Table 4,** with a single output instruction at the end of the loop. In fact, a 16-tap FIR filter's code is shorter by three instructions and runs at 1.65 μsec per data point. To calculate a 16-tap FIR filter, the 68000 requires at least 1590 cycles per data point; the 68010, 1142 cycles. Assuming 10-MHz μPs, these cycle times translate to 159 and 114 μsec, respectively. The FIR-filter accelerator thus affords acceleration factors of 96 and 69 times over 68000 μPs, respectively.

The FIR-filter accelerator described here is not a real-time digital filter. You could, however, adapt the design to real-time processing by adding an interface to new data through a 3-state latch (or FIFO buffer) to the local data bus. The data-acquisition subsystem would be responsible for ensuring that the latch is always ready with fresh data when the accelerator needs it. An easy way to update the RAM would be to use the post-incremented data-read address at the end of the loop as the write address to RAM. In operation, the FIR-filter accelerator would update RAM with this data at the end of each loop. **EDN**

References

1. Windsor, Bill, and Toldalagi, Paul, "Simplify FIR-filter design with a cookbook approach," *EDN*, March 3, 1983, pg 119.

2. Johnson, Matt, "Implement stable IIR filters using minimal hardware," *EDN*, April 14, 1983, pg 153.

Author's biography

David Fair is a marketing specialist in the DSP division at Analog Devices Inc (Norwood, MA). Employed at ADI for 3½ years, he previously worked at the Strategic Planning Institute in Cambridge, MA, and taught at the University of Vermont at Burlington. David has a BA in physics from Pomona College (Claremont, CA) and a PhD in the philosophy of mathematics, logic, and physics from Princeton University. His leisure-time activities include hiking, cycling, jogging, and windsurfing.

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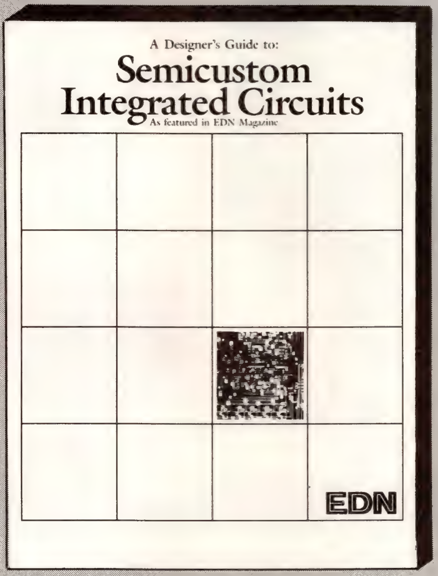

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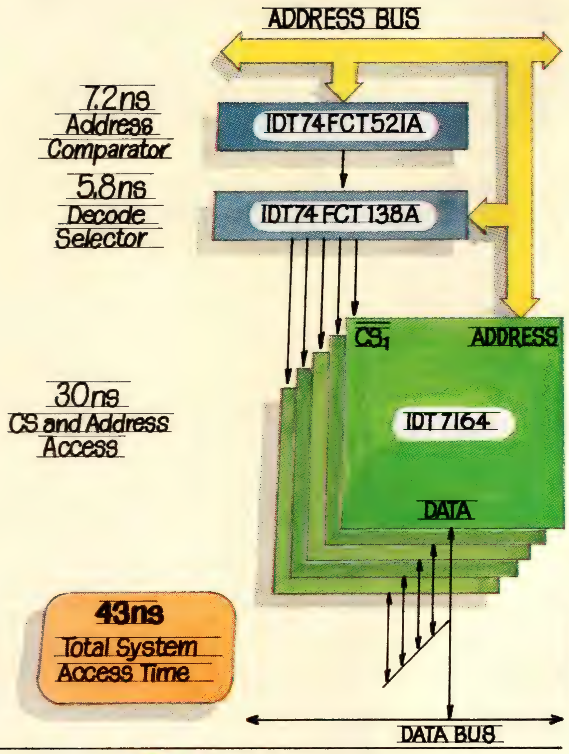

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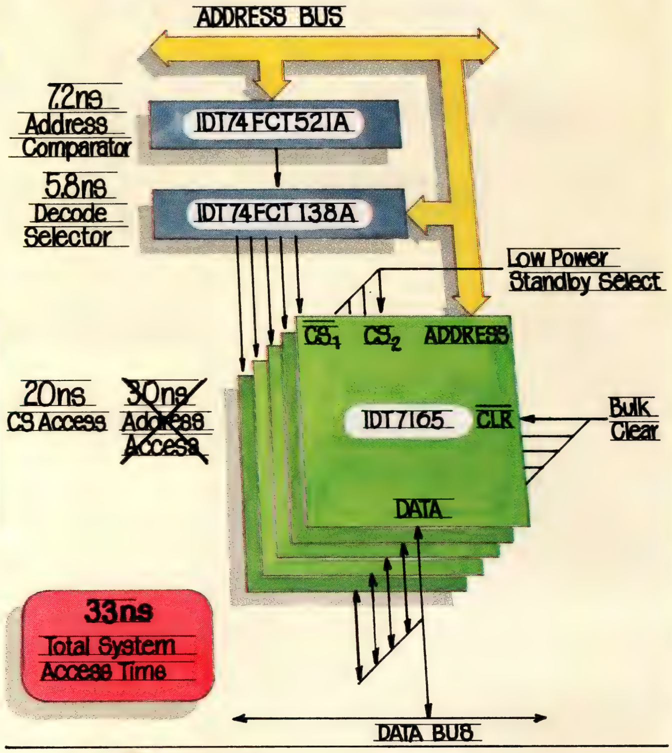

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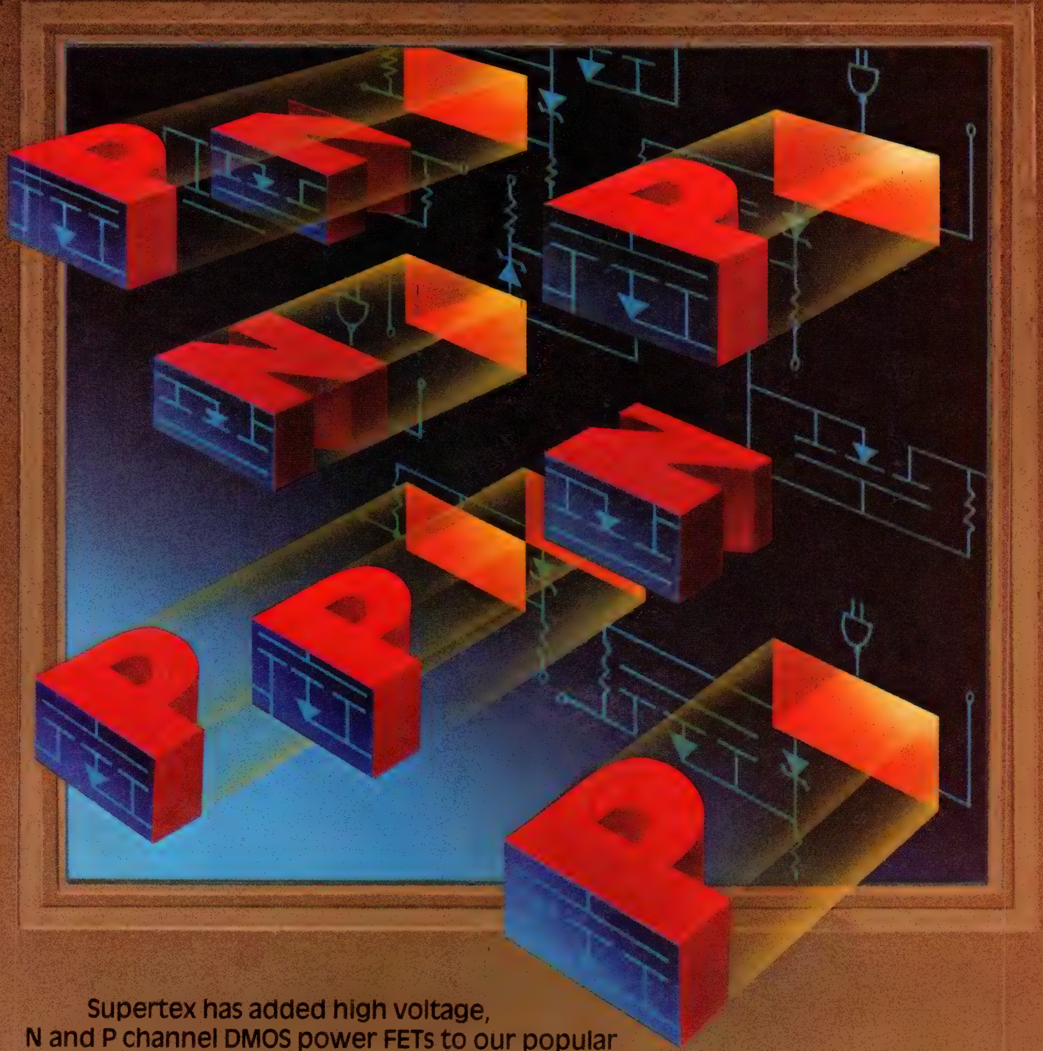

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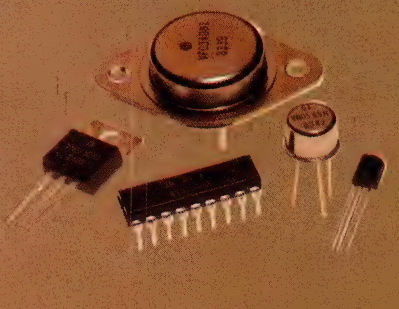

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CIRCLE NO 171

Created by Dayner/Hall, Inc., Winter Park, Florida

Compressing data conserves memory in bit-mapped displays

Most bit-mapped information is highly redundant; storing every pixel of such information wastes memory. You can save storage space and speed data-transmission rates in bit-mapped workstations by using a chip that employs standard CCITT algorithms to compress data.

Peter M Fuchs, *Advanced Micro Devices*

Because of recent developments in display systems, bit-mapped displays have replaced ASCII character-type displays in CAE workstations. Bit-mapped data, however, requires more image memory and a longer transmission time than does ASCII-encoded alphanumeric data. For example, a standard 8½×11-in. page displayed with a resolution of 300 lines/in. requires about 1M bytes of bit-mapped display memory. Likewise, you must transmit 1M bytes of data for the bit-mapped display instead of the approximately 4k bytes required for a page of alphanumeric characters.

To save storage space and speed data-transmission rates in bit-mapped workstations, you can take advantage of data-compression and -expansion techniques. By judiciously using these techniques, you can speed data transfers between workstations and facsimile machines and reduce storage requirements for bit-mapped images.

Designing a bit-mapped workstation

To design a bit-mapped system that operates with compressed data, you must first learn about the data-compression algorithms (see **box,** "Data-compression algorithms remove redundancy"). However, such a design needn't be complex. A typical computer system or workstation can use an Am7971 compression/expansion processor (CEP) chip (see **box** "The compression/expansion processor chip") to perform the necessary compression and expansion operations. Although the Am7971 addresses as many as 16M bytes of memory, a small computer may require only 1M bytes of system memory. In a typical system, an 80186 CPU chip lets you configure a basic interface to the CEP. The 80186 host CPU also lets you add other peripheral chips to the display system.

The CPU chip transfers register-control information directly to and from the CEP chip, treating the CEP as a slave processor. To assist in controlling I/O devices, the 80186 chip supplies five peripheral chip-select (PCS) signals that function under program control. In the display-controller circuit **(Fig 1)**, the 80186's $\overline{PCS3}$ output controls the CEP's chip-select input line, $\overline{CS}$.

Text continued on pg 178

Data-compression algorithms remove redundancy

To encourage the use of compressed data, the CCITT established a set of recommended standards for group 3 and group 4 digital facsimile transmissions. For example, group 3 facsimile devices operate over standard phone lines, and they transmit an 8½×11-in. page of graphic and text information in 1 minute or less. The minimum vertical resolution is 100 lines/in., and the minimum horizontal resolution is 1728 picture elements (pixels). The group 3 algorithm compresses data in one dimension (1-D) by removing horizontally redundant pixels. An optional 2-dimensional (2-D) mode lets you also remove vertically redundant information. Group 4 compression provides a 400-pixel/in. 2-D compression mode.

The CCITT algorithms remove redundant information by using one of two codes: a 1-D modified Huffman code or a 2-D modified relative-element address-designate (READ) code. The Huffman-code algorithm calculates a line-length value that represents the number of consecutive pixels of the same color —black or white—in a horizontal scan line across the document. The algorithm converts the count into a run-length code. The algorithm continues by counting the next pixel group of the other color and assigns a code to the new count. The Huffman algorithm assumes that all scan lines will start with at least one white pixel. So, when a scan line actually starts with a black pixel, the compressor sends the code for a zero-length line of white pixels.

To save memory space and transmission time, Huffman-code words have variable lengths. Line lengths that occur often in a document produce a shorter code word than lengths that occur less frequently. Unique codes define black and white lines that contain 0 to 63 pixels. When it encounters a longer line, the compressor breaks the line into 64-pixel lengths and sends a code for the number of complete lengths. Any remainder that contains fewer than 64 pixels generates a unique code. For example, a line of 1700 pixels is encoded by concatenating the code word for 1664 (26×64) and the code for the remainder, 36. Because the length of a code word ranges from two to as many as 12 bits, encoders are difficult to implement with SSI and MSI logic.

When you use the 1-D Huffman algorithm to compress eight CCITT-standard documents, the compression ratios vary between 5:1 and 15:1. The ratio is the number of pixels divided by the number of code bits. Because the compression ratio depends on how much redundant information the algorithm removes from a document, the ratio depends on the type of document—drawing, schematic, text—and the resolution you scan it with.

2-D codes are relative

The 2-D compression algorithm employs the READ code. The READ-code algorithm encodes a scan line based on the position of color changes in the previous scan line, which serves as a reference. When a color change in the newly scanned line lies exactly below the same color change in the reference line, a single code bit represents the change. Other codes indicate color changes in the encoded line that are no farther than three pixels from the corresponding color change in the reference line. When color changes in adjacent lines exceed three pixel positions, the compressor generates a special code and then represents the distance as a 1-D code. Encoding the eight CCITT-standard documents with the 2-D READ code yields compression ratios of between 7:1 and 50:1.

A pass-mode condition exists when the reference line contains a color change but a portion of the encoded line below it doesn't. A unique code identifies the pass-mode condition. To overcome the need for a reference line at the start of a READ-code transmission, you can either send the first line encoded in 1-D code, or you can assume the reference line is white.

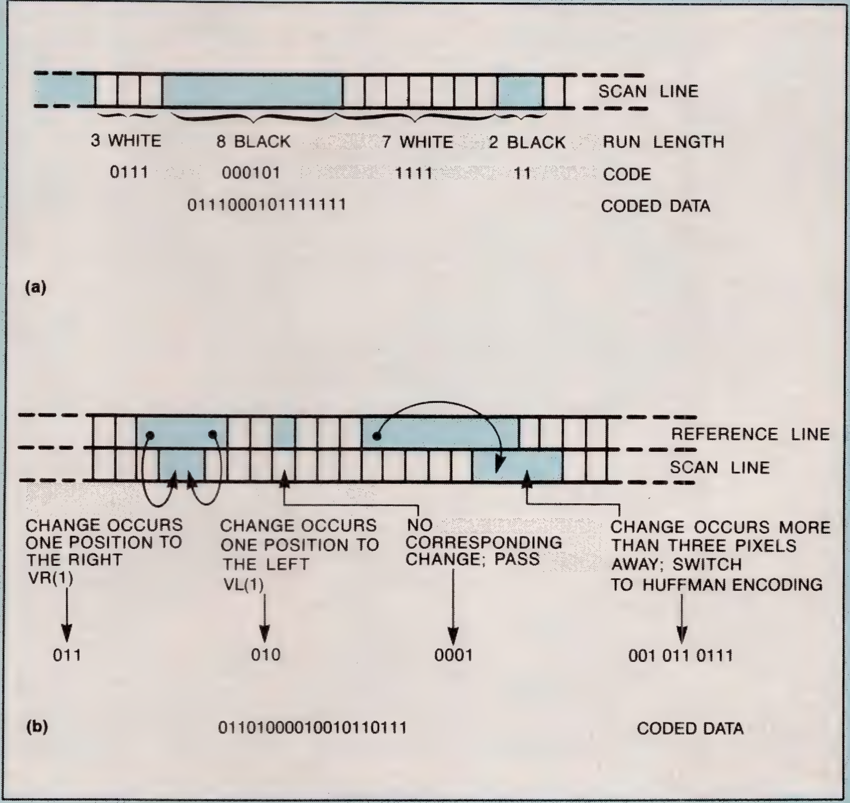
Although 2-D encoding offers higher compression ratios than does 1-D encoding, it has disadvantages. For example, the 2-D encoding computer or logic circuit must temporarily store a reference line. Therefore, systems that get data from a line scanner and directly compress it require complicated memory configurations. Also, an error in a 1-D code affects only one display line, but such an error propagates through an entire 2-D-encoded document.

K parameter blocks errors

To assist in recovering from an error, the Huffman and READ codes also provide user-selectable parameters such as K. The K parameter sets the number of scan lines encoded in 2-D mode before the compressor sends one scan line encoded in the 1-D mode. When the compressor sends a 1-D-encoded line regularly, any 2-D errors run through a maximum of K lines.

An end-of-line code also improves a compression/expansion system's error-detection capability. Because a scan line's length is known, you can decode an encoded line and reconstruct the scan line on your display without a delimiter that signifies the end of a scan line. However, if you include end-of-line codes in the encoded scan-line information, the receiving system can detect when the display's line length and the number of pixels received don't match.

Complicated pictures such as half-tone images may yield an encoded block of data that exceeds the length of the original image data. To avoid such negative compression, the compressor inserts a code in the transmission to indicate that uncompressed data follows. However, before transmitting the uncompressed data, the compressor must filter out any bit patterns that match escape-code sequences that perform special control operations in the receiving unit. Mixing encoded and unencoded data lets you keep a transmission as short as possible.


SCAN LINE
3 WHITE
8 BLACK
7 WHITE
2 BLACK
RUN LENGTH
0111
000101
1111
11
CODE
0111000101111111
CODED DATA
(a)
REFERENCE LINE
SCAN LINE
CHANGE OCCURS ONE POSITION TO THE RIGHT VR(1)
CHANGE OCCURS ONE POSITION TO THE LEFT VL(1)
NO CORRESPONDING CHANGE; PASS
CHANGE OCCURS MORE THAN THREE PIXELS AWAY; SWITCH TO HUFFMAN ENCODING
011
010
0001
001 011 0111
(b)
01101000010010110111
CODED DATA

***Encoding a scanned line** with a 1-D algorithm **(a)** involves counting groups of pixels in a scan line and assigning the equivalent codes to the counts. The algorithm concatenates the codes to form a complete code that represents the scan line. The 2-D algorithm **(b)** relates the new scan line to the color changes in the previous line. When changes are more than three pixels apart, the encoder switches to modified Huffman codes.*

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The compression/expansion processor chip simultaneously encodes and decodes image data in 1-D or 2-D formats.

When the CEP's $\overline{CS}$ input is logical zero, its bus transceivers connect the chip to the 80186's least-significant data-bus lines.

The CEP can, in turn, control the 80186 by adding wait states to its memory-access cycles. By gating the CEP chip's Ready signal and its $\overline{CS}$ input, you generate a control signal that drives the CPU chip's asynchronous-ready input, ARDY. Whenever the CPU chip drives the CEP's $\overline{CS}$ input to logical zero, the CPU must wait while the CEP processes information. Because only the CEP chip controls the CPU's ARDY signal, memories and other peripherals must operate without wait states.

CEP performs DMA operations

When the CEP must perform a DMA transfer, it asserts its hold-request output (HRQ). Because the CEP is the only device that performs DMA-transfer operations in the circuit, its HRQ line controls the CPU's HRQ input directly. Systems with additional DMA-type peripherals will require bus-request arbitration logic. After detecting the HRQ signal from the CEP chip, the CPU asserts its hold-acknowledge output (HLDA), thereby signaling the CEP that the bus is free for DMA operations.

When the CPU asserts the HLDA signal, the Am29867 transceiver passes CEP address lines A_7 to A_0 through to the computer's system-control bus. Address buffers or transceivers aren't necessary for CEP address lines A_8 to A_{15} because the CEP puts these lines in a high-impedance state when it isn't using the bus. An Am29848 3-state latch holds the three MSBs of the memory adress, A_{16} to A_{19}, which arise from the CEP chip's multiplexed address-data bus, AD_{16} to AD_{23}.

Although the 80186 transfers information as 16-bit values, the CEP operates on bytes. It's necessary,

Text continued on pg 182

The compression/expansion processor chip

The Am7971 compression/expansion processor (CEP), which adds image bit-boundary processing to the original Am7970, handles both the compression and the expansion of bit-mapped data. You can program the chip to generate and accept K-parameters, end-of-line codes, byte-boundary-fill bits, and other options, such as time-fill bits. The CEP detects a negative-compression condition and generates an interrupt that goes to the CEP's host computer.

The CEP operates with two memory sections: source and destination memory. During an expansion operation, the source memory contains encoded data, and the destination memory contains the decoded data for the system's bit-mapped display or printer. When the chip operates in its 2-D mode, the destination memory stores the reference-line bits. During compression operations, the source memory contains the display's bit map and the destination memory contains encoded data. The source memory stores the reference line during 2-D compressions.

The CEP provides two separate control buses; a system bus and a document bus. Both buses furnish 24 address bits multiplexed with eight data bits. Because the chip has a built-in DMA controller, it can access the host CPU's main memory without requiring the CPU to execute a special data-transfer program. Hold-request and hold-acknowledge handshaking signals control the DMA operations.

The chip's document bus controls the memory that holds unencoded image data. Because the amount of raw document data that the chip operates on is large, the CEP's performance is highest when it alone uses the bus. Therefore, the document bus doesn't provide any handshake signals that would control bus arbitration for several devices. If you want an external device to access the document memory, you must supply extra bus-arbitration logic.

Depending on how you program the chip's internal command registers, your system may contain separate destination and source memories, one on each of the chip's two memory-control buses. Because the CEP chip's expander and compressor circuits work independently, the chip can compress one document while simultaneously expanding another. Alternatively, you can program the chip so that it controls both memories on only one bus. However, the single-bus configuration slows the compression/expansion tasks because it precludes simultaneous compression and expansion operations.

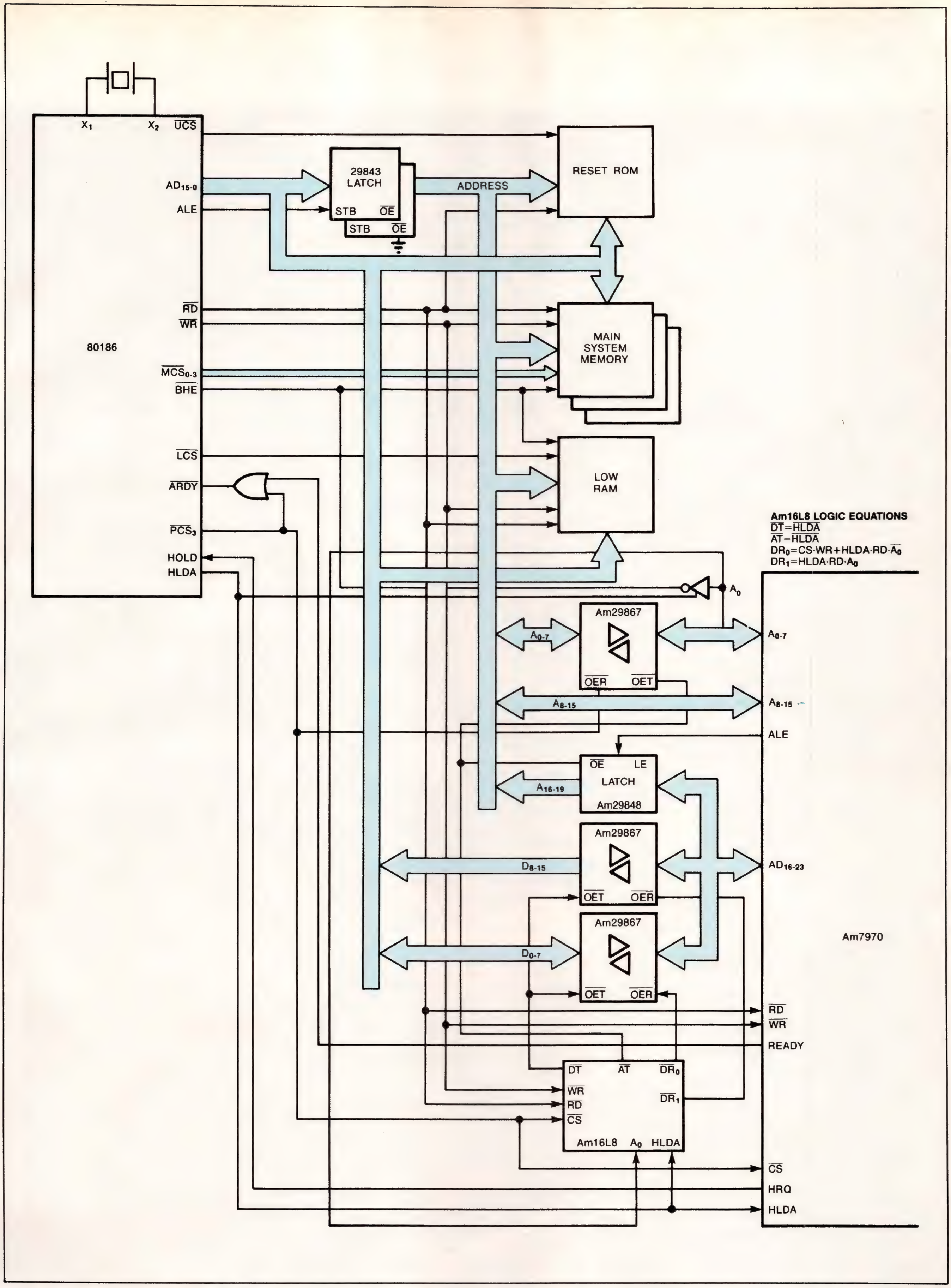

Fig 1—The CEP system bus *links the compression/expansion-processor (CEP) chip and the host μP chip. The CEP has access to the main-system memory when it initiates a DMA operation. The Am16L8 supplies the proper control signals to the CEP's bus buffers and transceivers.*

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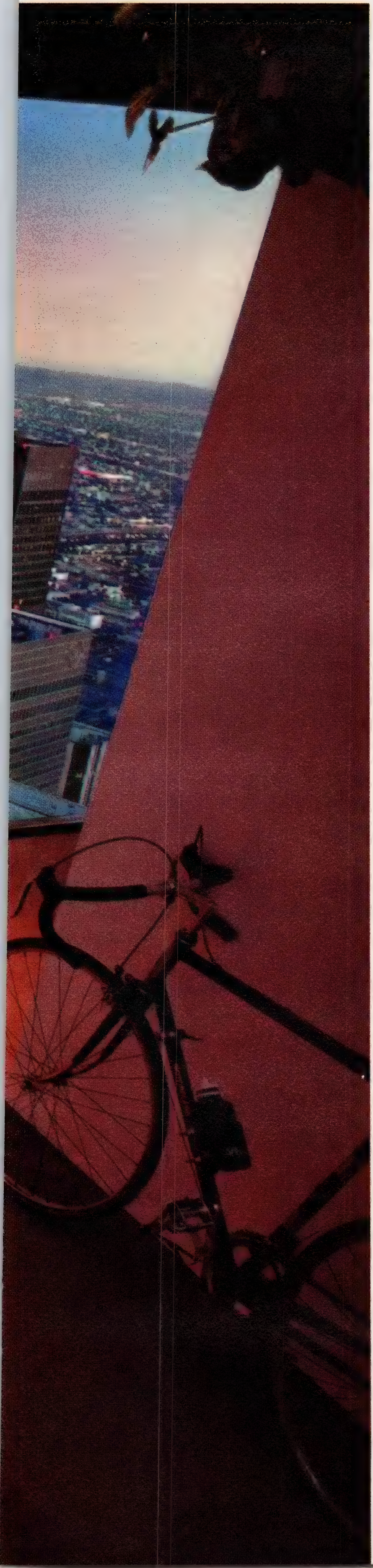

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Huffman and READ codes remove redundant information from graphic and text information.

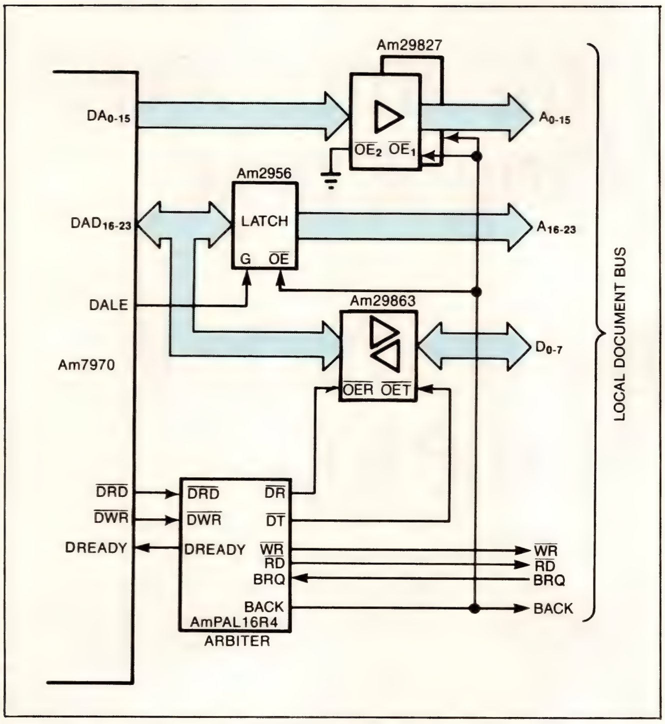


Fig 2—The CEP's local document bus *lets the chip control its own memory. If other devices must access the document memory, you'll need arbitration logic, bus latches, and bus transceivers that let each device use the bus in turn.*

therefore, to transfer bytes from the 80186 to the CEP and, conversely, to transfer words from the CEP to the 80186. Two Am29867 transceivers perform the bus-sizing operations that transfer information between the chips. For example, address bit A_0 governs whether a high or a low byte is involved in read or write operations. To provide the system bus with the same signals the CPU provides, the A_0 signal also provides a bus-high enable (BHE) signal that controls byte- and word-transfer operations over the data bus. A programmable-logic device (Am16L8) controls the transceivers and latches.

Because the CEP's document bus is a high-speed, low-overhead bus, it doesn't provide bus-arbitration signals the way the system bus does. However, another device might need to access the document memory. For example, a page scanner would transfer pixel information to the CEP's document memory in preparation for a compression operation. Also, a CRT controller might display the bit map's information on a screen. Such a system requires a bus-arbitration circuit **(Fig 2)**, which you can construct from a state machine built around an AmPAL16R4 **(Fig 3)**. The complete bus-arbitration circuit also provides a 24-bit address bus and an 8-bit data bus.

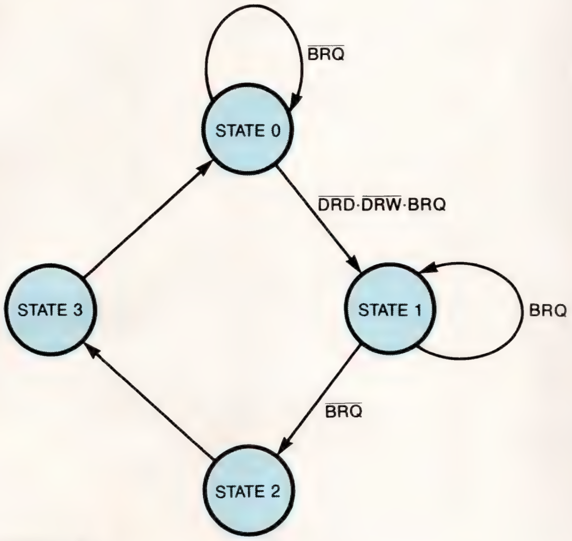
When the bus-arbiter PLD receives a bus-request signal (BRQ) from the master, it tests the CEP's $\overline{RD}$ and $\overline{WR}$ lines. If either line is active, the arbiter waits for the CEP to complete its bus-access cycle. After the CEP completes its cycle, the arbiter asserts the CEP's Ready input, thereby preventing the chip from accessing the bus. The bus arbiter also asserts its BACK output, disabling the CEP's bus drivers and transceivers and signaling the master that the bus is available.

Arbiter controls bus access

As soon as the master releases the bus and drives the BRQ signal to logical zero, the bus arbiter re-enables the CEP's drivers and transceivers. If a CEP bus-access operation is waiting, the bus arbiter waits one clock cycle and then generates the necessary read or write signal. The 1-clock delay provides the same address-setup timing as that found in a CEP-based system that lacks any bus-arbitration logic. One clock cycle after it activates the read or write line, the arbiter asserts the Ready input so the CEP can complete the memory-access operation. The arbiter does not let the CEP insert wait states in memory-access cycles, so the document-storage memory must be fast, fetching or storing data within one clock cycle.

After completing the interface design, you must consider how you want to program the CEP, because the Am7971 offers a variety of options for compression and expansion. After you apply power to the CEP, a reset forces the CEP into an idle state, which clears all its internal registers. The CPU then programs the processor by loading the chip's internal registers with information. For compression and expansion processes, you must specify the starting addresses for the blocks set aside for the source and destination memories. You must also specify the size of the source and the destination memories. During expansion operations, the two values are known in advance. The size of the source memory equals the size of the data file that has to be expanded, and the destination memory is the same size as the display's bit map.

Setting memory sizes for compression operations is more complicated. The source memory, which you know, is the size of the bit map. However, the size of the destination memory depends on the compression ratio, a value you don't know before compressing the data. You could assume the worst case—a compression ratio of one—and assign the destination the same space as



OUTPUTS:

BACK=STATE 2

DREADY=STATE 0

$\overline{WR}$: IF($\overline{STATE\ 1}$)$\overline{WR}$=STATE 2+STATE 3·$\overline{DWR}$+STATE 1·$\overline{DWR}$

$\overline{RD}$: IF($\overline{STATE\ 1}$)$\overline{RD}$=STATE 2+STATE 3·$\overline{DRD}$+STATE 1·$\overline{DRD}$

$\overline{DT}$=STATE 1+$\overline{DWR}$

$\overline{DW}$=STATE 1+$\overline{DRD}$

Fig 3—The state-machine for the bus arbiter *resides in an AmPAL16R4. That chip controls the memory-read and -write signals as well as the bus-request and bus-acknowledge signals.*

the source memory. But you can try a smaller memory block first, if you wish; the CEP will generate an interrupt if the compressed data exceeds the memory space you assign it. After detecting such an interrupt, the host computer can expand the destination memory or it can save the compressed data (on a disk, for example) and then restart the CEP.

The Go bit starts the chip

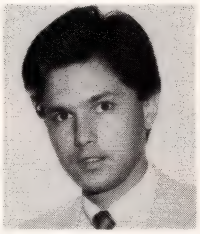
Before using the CEP, you must select the compression method (1-D or 2-D) and any options to be used. Setting the Go bit in either the compressor's or the expander's master-control register starts the CEP. Setting both Go bits causes simultaneous compression and expansion operations. The CEP sets a busy-status bit in the compressor-status register (CSR) or the expander-status register (ESR) when it performs each type of operation. The busy-status bits are also available in the master-status register (MSR).

Whenever one of the busy-status bits changes to the not-busy state, the CEP generates an interrupt that alerts the host computer. The host must then examine the status bits in the MSR to determine whether the compressor or expander caused the interrupt. Computers that poll I/O devices instead of responding to interrupts must test the busy-status bits in the CEP's status register frequently to detect any changes.

To determine the cause of an interrupt, the host computer reads the interrupting processor's status register. For example, when the expander causes an interrupt, the CPU checks the source- and the destination-overflow bits. If one of these bits is set and if the line-processing-incomplete bit is set, an error has occurred, and the host computer must take necessary steps to recover and continue processing data.

Another condition that can cause an interrupt is a data error, which the CEP detects only when it uses end-of-line codes. Because the number of pixels per line is preset in the CEP by the host computer, the CEP knows when to expect an end-of-line code. Thus, if the CEP receives an end-of-line code at the wrong time, it generates an interrupt. After receiving the interrupt, the host computer attempts to recover from the error by reprocessing the line of data. **EDN**

Author's biography



Peter M Fuchs is a product-planning engineer who develops office-automation products at Advanced Micro Devices Inc in Sunnyvale, CA. He received his diploma from the Swiss Federal Institute of Technology (Zurich) in 1984. Peter enjoys swimming and windsurfing, and he teaches digital-design classes for the extension program at the University of California at Berkeley.

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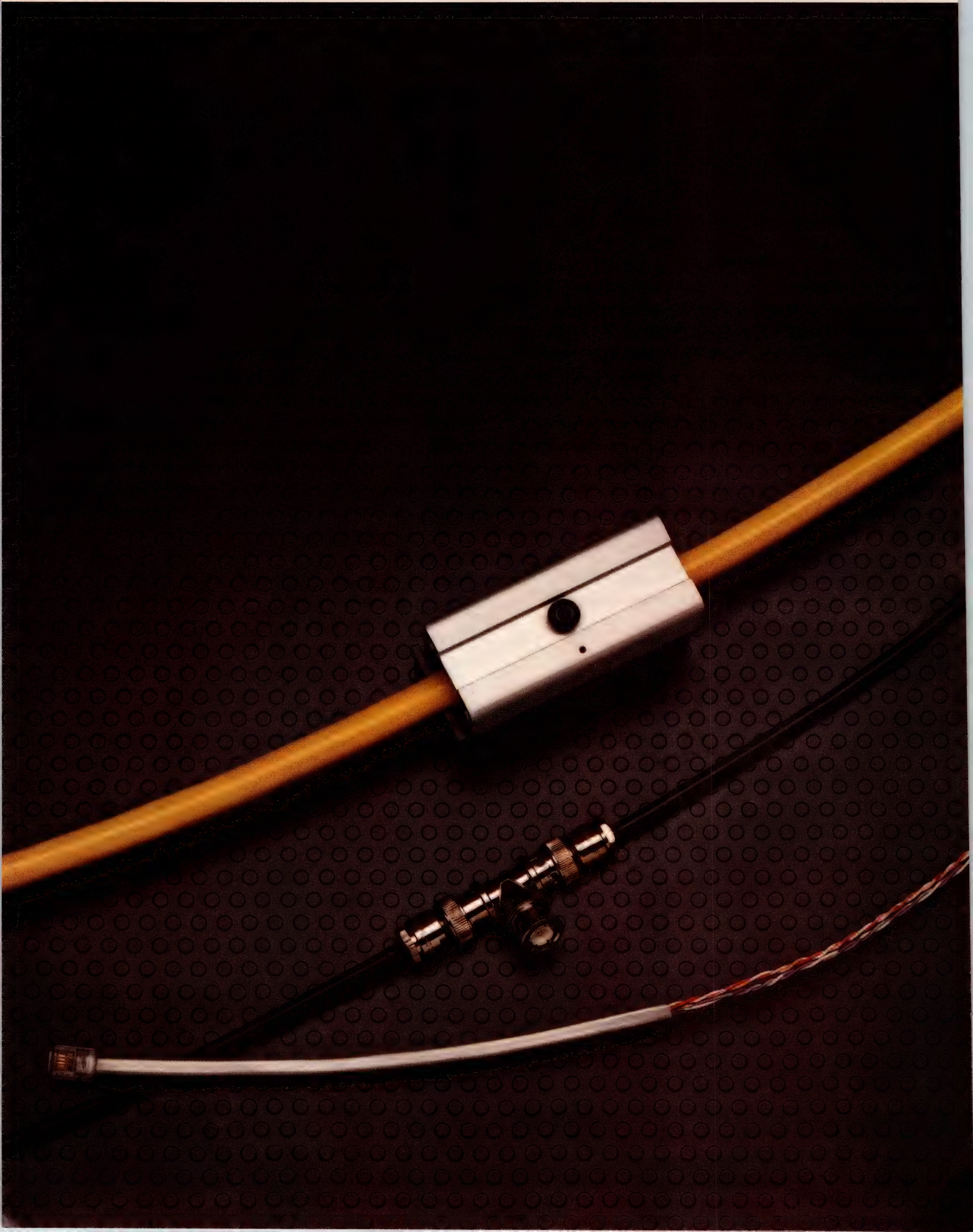

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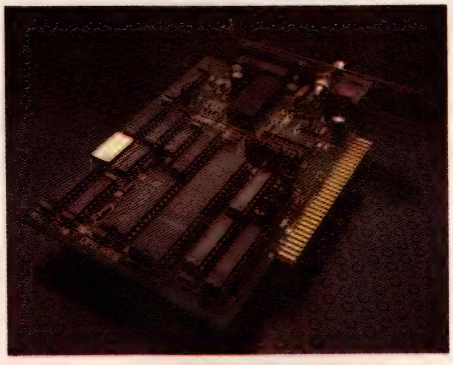

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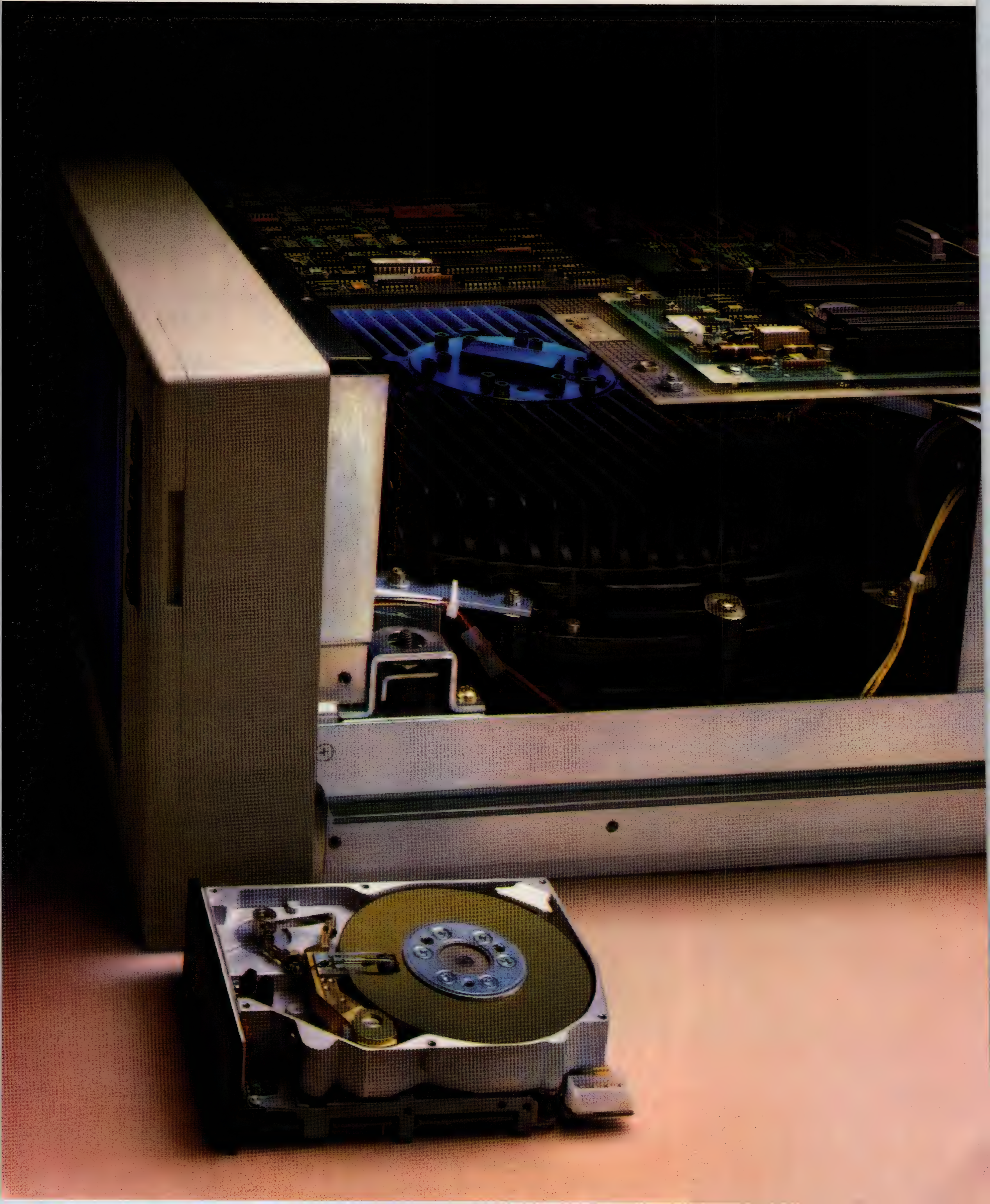

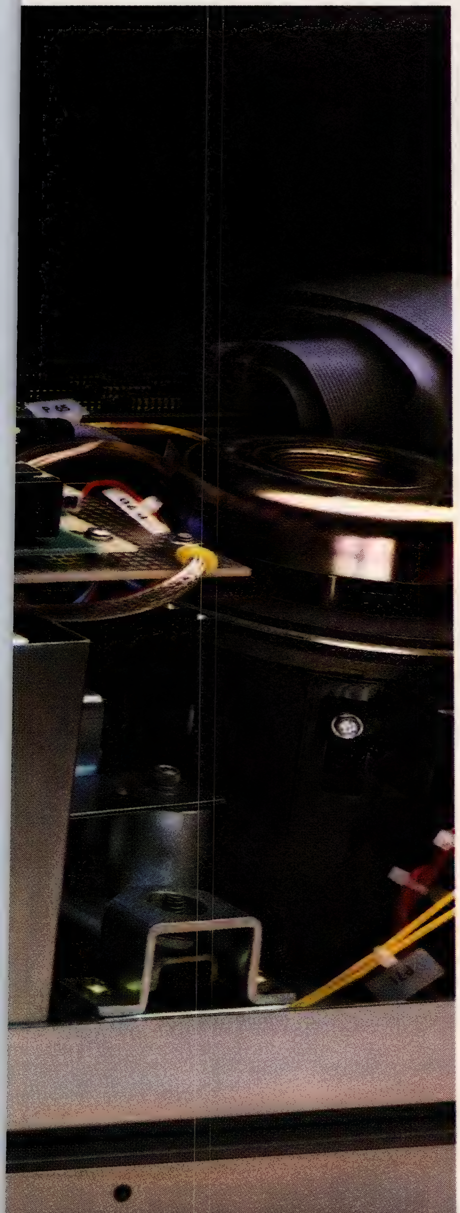

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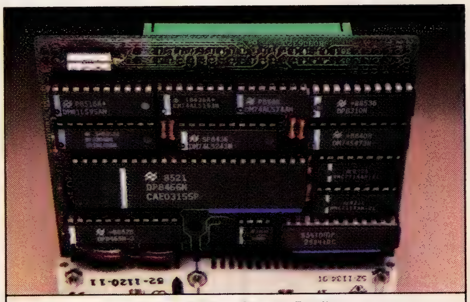

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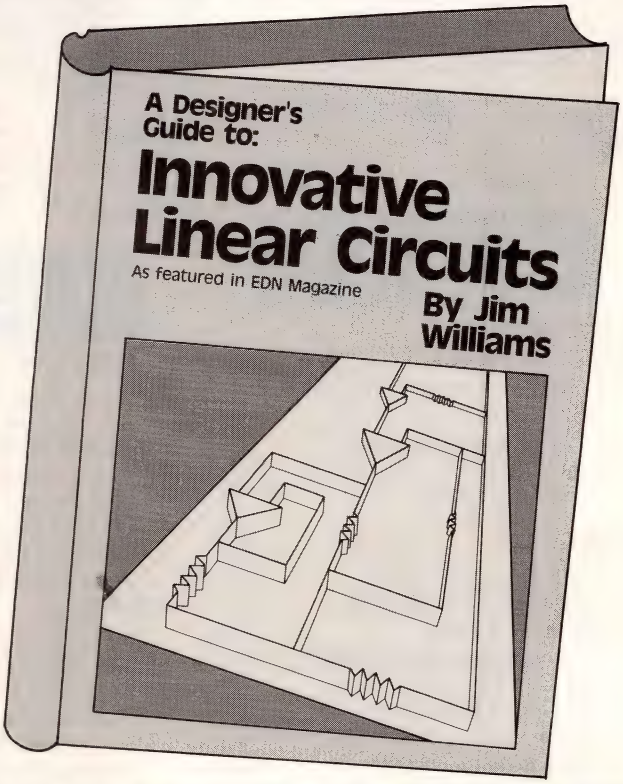

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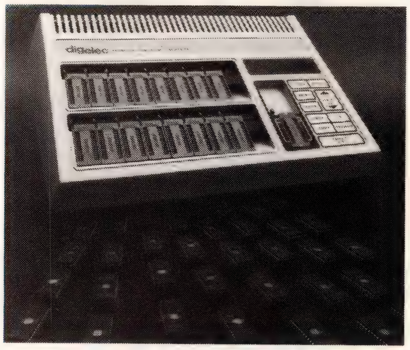

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27256	185	50	151	135
27512	385	110	325	280

*1 = Intelligent   2 = Quick-Pulse

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Programming schemes change applications role of EPROMs

Fast programming algorithms, gang programmers, and device-handling equipment allow OEMs to maximize EPROM-programming yields while still getting end products to market quickly.

Denise Slocombe, *Data I/O Corp*

The EPROM, which was once merely an engineering-design tool, is now widely used in place of masked ROM as a low-cost production part. Developments such as fast programming algorithms, gang programmers, and device-handling equipment have cut the overall programming time for today's high-density EPROMs to a minimum, thus maximizing EPROM-programming yields in the production area and keeping finished-product and inventory costs to a minimum.

When EPROMs were first introduced, they were used primarily as engineering-design tools for generating and debugging program code targeted for eventual installation in a masked ROM. It was easy to program and install EPROMs in the equipment for testing and evaluation. In short, the EPROM let the designer thoroughly test the firmware code and fix bugs without the expense and long leadtimes that tooling new masked ROM would incur. Although the EPROM had a relatively high unit cost, that cost was not a problem in the engineering-design environment. The cost was, however, significant enough to prevent many OEMs from shipping EPROMs in high-volume products.

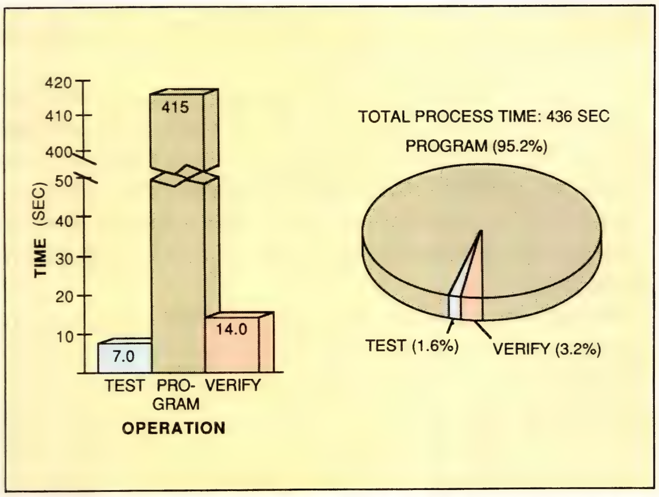


Fig 1—EPROM-programming time is much longer *than test and verify times when you use the standard 50-msec algorithm. (The times shown here are for a 2764 EPROM programmed with the 50-msec algorithm.)*

As the unit cost of the EPROM dropped, however, manufacturers found they could afford to use such devices in place of masked ROM in many applications. By using an EPROM, an equipment manufacturer could put a product on the market quickly, because the leadtime associated with the masked ROM would be eliminated.

The increased manufacturing levels required a volume of EPROMs that overburdened standard manual programming units, however. Manufacturers of programming equipment solved the programming-bottleneck problem by making device-handling equipment and gang programmers. Device-handling equipment automatically loads, programs, and unloads single

> *To realize the highest device yields in a production environment, you must use the correct programming algorithm.*

EPROMs one after the other. Gang (or parallel) programmers can simultaneously program a number of devices.

Device-programmer companies also took advantage of the fast programming algorithms developed by EPROM makers. These algorithms allowed the programming of high-density EPROMs to take place within a reasonable amount of time. A programming algorithm is a collection of device-dependent parameters, supplied by the EPROM manufacturer, that specify the exact voltage levels to apply and when and where to apply them, the length of the programming pulse, and the voltage rise times.

Different types or brands of EPROMs usually require different programming algorithms. For example, several manufacturers provide the widely used 2764 EPROM. Although these parts operate identically in a circuit, you must use different algorithms to program the various devices **(Table 1).**

To realize the highest device yields in a production environment, you must use the correct programming algorithm. If you use an incorrect algorithm, you may make the EPROM manufacturer's reliability assurances void, and the chances are good that you'll reduce the number of devices that you can successively program from a given lot.

When you consider the overall EPROM-programming process, you must also consider the testing and verification operations. By testing the part before the programming operation takes place, you can ensure that the part is inserted correctly in the programmer socket, that no bits are set that would prevent proper data programming, and that the part is functionally capable of being programmed. You save a good deal of time by testing before programming rather than after.

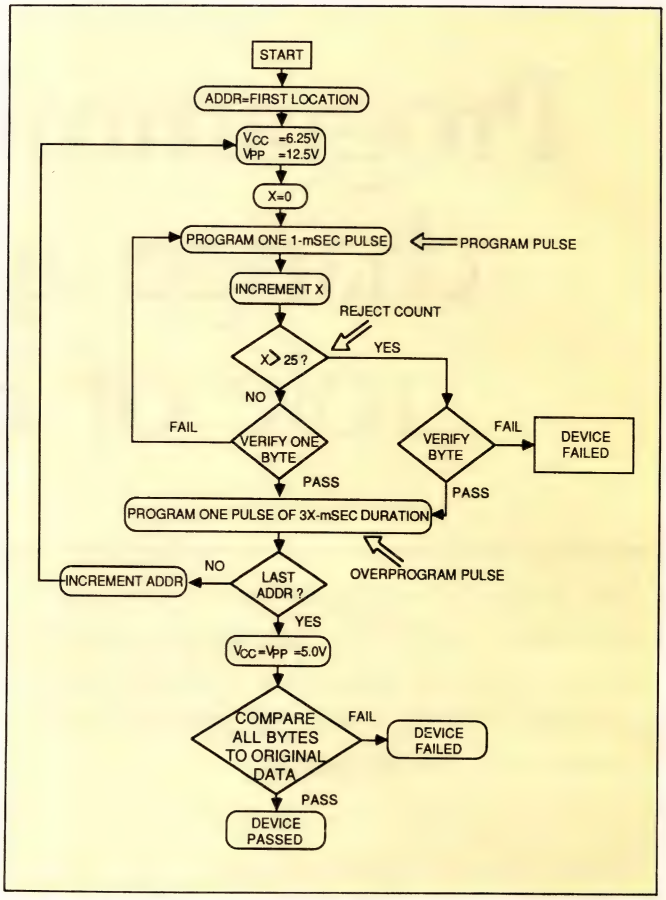


***Fig 2—To decrease programming time,** Intel's Inteligent algorithm replaces the single long pulse with shorter programming pulses. This flowchart shows the operation of the algorithm.*

For many EPROMs (particularly earlier versions), the programming sequence typically proceeds as follows. You address the first memory location and apply the code to the data inputs. You then apply a program-

TABLE 1—PROGRAMMING ALGORITHM PARAMETERS

ALGORITHM PARAMETER	INTEL 2764	INTEL 2764A	INTEL P2764A	AMD 2764	AMD 2764A	FUJITSU 2764/C64
V_{CC}	6V	6V	6.25V	6V	6V	6V
V_{PP}	21V	12.5V	12.75V	21V	21V	21V
PROGRAM PULSE	1 mSEC	1 mSEC	100 μSEC	1 mSEC	1 mSEC	1 mSEC
OVERPROGRAM PULSE	4X	3X	0	2 mSEC	2 mSEC	1X
REJECT COUNT	15	25	25	25	25	20

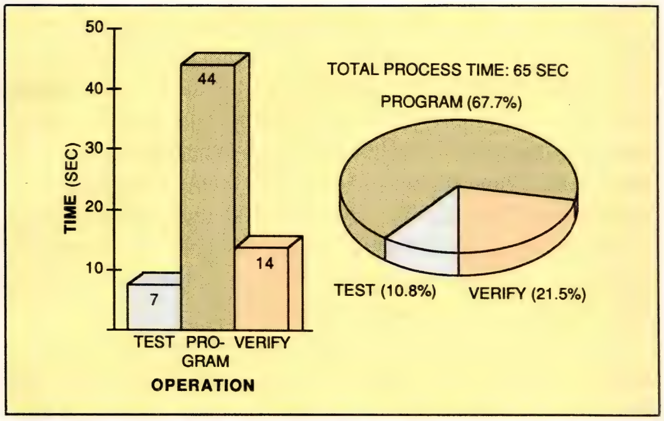


*Fig 3—**Although the Inteligent algorithm significantly reduces programming time** over that obtained with the standard 50-msec algorithm, it has no effect on the test and verify times.*

ming pulse to a specified pin for a specified period of time. Then you repeat these two steps for each of the remaining memory locations until you've programmed the entire part.

The verify operation checks to make sure the code programmed into the EPROM matches the code stored in the programmer. To make this check, the verify operation reads each byte of each part and compares the data with the master part, or with the master data stored in the programmer's RAM. Failure to find a match results in a verify-error indication.

Historically, EPROMs like the 2764 typically required a relatively long (50-msec) programming pulse to ensure that each address location was truly being programmed. As a result, the programming time was much greater than the time required for test and verification **(Fig 1).** As you can see from the pie chart, the test and verify times are comparatively short, so they don't contribute significantly to the total time required to program the part.

As EPROM capacities increase, however, such long programming times are no longer acceptable. The time it takes to program an EPROM varies in a direct relationship with the number of bits. To decrease programming times and improve parts yields, today's large-capacity (greater than 8k bytes) EPROMs and EPROM programmers use intelligent algorithms.

Intelligent algorithms use shorter programming pulses instead of a single long pulse. **Fig 2** gives a flowchart for Intel's Inteligent programming algorithm. Instead of first programming all bytes and then going back to test all the bytes, this algorithm tests each byte immediately after applying the pulse to verify that it is correctly programmed. The net result is an improvement in programming speed **(Fig 3).**

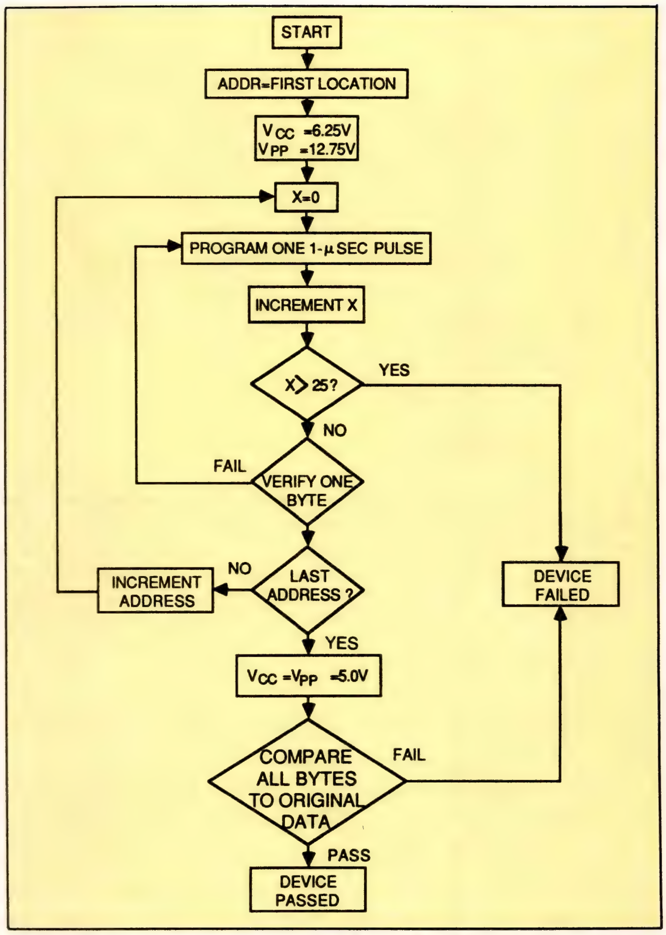


*Fig 4—**To improve programming throughput,** Intel's Quick-Pulse Programming algorithm uses 100-μsec programming pulses. Although it's similar to the Inteligent algorithm, the Quick-Pulse algorithm uses no overprogram pulse.*

Fig 3 also shows that the test and verify times for EPROMs programmed with the intelligent algorithm match those for EPROMs programmed with the 50-msec algorithm **(Fig 2).** When you use the 50-msec algorithm, the test and verify times account for only 4.8% of the overall programming time; when you use Intel's algorithm, they account for a full 32.3% of the programming process. Note, however, that for the same 2764 EPROM, the intelligent algorithm does reduce overall programming time from 436 to 65 sec.

Of course, when you increase EPROM-programming throughput, you reduce the fabrication costs of your end product. Simply put, programming throughput is a measure of the number of parts successfully programmed and verified in a given period of time. Programming time contributes significantly to overall

To decrease programming times and improve parts yields, today's large-capacity (greater than 8k bytes) EPROMs use intelligent algorithms.

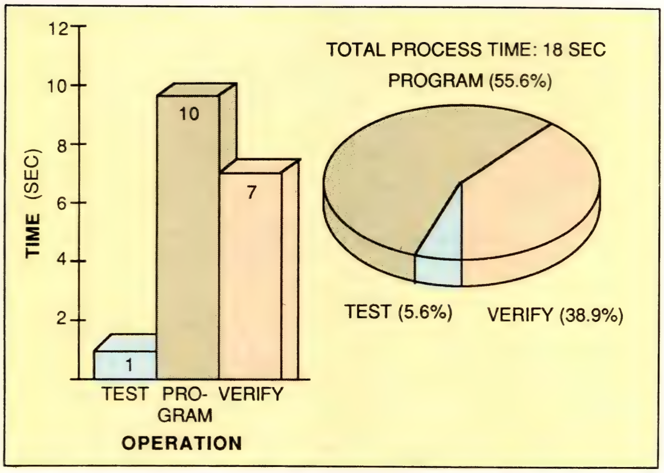


Fig 5—The operating overhead of your device programmer can slow your programming time *even when you use the Quick-Pulse algorithm. This figure illustrates the actual programming time for a 2764 EPROM programmed with the Quick-Pulse algorithm on the Data I/O Model 120 programmer, which has a 9.2-sec operating overhead. Even though you can theoretically program a 2764 in only 800 μsec, the programmer's overhead increases the programming time to 10 sec.*

EPROM cost. The longer the programming time, therefore, the more expensive the part.

Three main factors affect EPROM-programming throughput: the time required to insert and withdraw the part from the programming socket; the time required to test, program, and verify the part; and the programming yield, the number of parts that are successfully programmed.

When you consider how to increase programming throughput in your production area, you must decide whether to employ parallel or serial programming techniques. In the parallel technique, you manually load a number of EPROMs into a multisocket programmer, and then unload them after the programming operation. Obviously, the parallel approach greatly reduces the per-part programming time. However, the handling time (loading and unloading parts) is still in the range of 2 to 5 sec per part.

A mechanical handler facilitates the serial programming process. This piece of equipment automatically loads each EPROM so that the pins make proper contact with the programming socket. When the programming operation is complete, it unloads and sorts the devices according to the results (device pass, device fail, or data verification failure) of the test and verify operations. Although the automatic equipment reduces handling time, it does nothing to reduce the per-part programming time.

To decide whether parallel or serial programming is best for your purposes, you need to know the sum of the programming and handling times. **Table 2** lists the programming and handling times for 2764 EPROMs programmed with both the parallel and the serial methods, optimized programming equipment, and the Inteligent algorithm. Note that the per-part programming time obtained with the parallel technique is the total programming time divided by the number of parts in the programmer (30, in this case). The parallel

TABLE 2—PROGRAMMING THROUGHPUT (INTELLIGENT ALGORITHM)

P2764 EPROM	PARALLEL	SERIAL
PROGRAMMING TIME	1.2 SEC/PART (36 SEC FOR 30 PARTS)	36 SEC/PART
HANDLING TIME	2.5 SEC/PART	1 SEC/PART
TOTAL TIME (PER PART)	3.7 SEC/PART	37 SEC/PART
THROUGHPUT	973 PARTS/HOUR	97 PARTS/HOUR

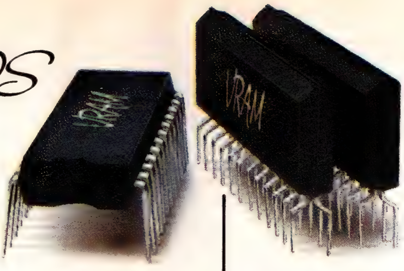
NOTE:
THE PARALLEL PROGRAMMING TIMES WERE OBTAINED WITH THE SERIES 1000 PARALLEL PROGRAMMER. THE SERIAL TIMES ASSUME A HYPOTHETICAL SINGLE-SITE PROGRAMMER WITH A SPEED EQUAL TO THAT OF THE SERIES 1000.

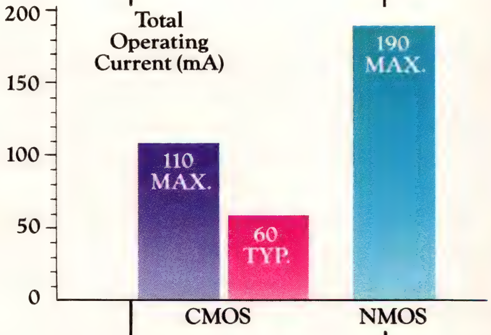
TABLE 3—PROGRAMMING THROUGHPUT (QUICK-PULSE PROGRAMMING ALGORITHM)

P2764A EPROM	PARALLEL	SERIAL
PROGRAMMING TIME	0.05 SEC/PART (1.4 SEC FOR 30 PARTS)	1.4 SEC/PART
HANDLING TIME	2.5 SEC/PART	1 SEC/PART
TOTAL TIME (PER PART)	2.55 SEC/PART	2.4 SEC/PART
THROUGHPUT	1412 PARTS/HOUR	1500 PARTS/HOUR

NOTE:
THE PARALLEL PROGRAMMING TIMES WERE OBTAINED WITH THE SERIES 1000 PARALLEL PROGRAMMER. THE SERIAL TIMES ASSUME A HYPOTHETICAL SINGLE-SITE PROGRAMMER WITH A SPEED EQUAL TO THAT OF THE SERIES 1000.

The Mitsubishi 120ns CMOS Video RAM





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M5M4C264P-15	64K x 4	150ns	60ns	24 pin DIP
M5M4C264L-15	64K x 4	150ns	60ns	24 pin ZIP

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*Zig-Zag In-Line Package
Graphic image courtesy of Computervision Corp.

CIRCLE NO 125

EPROM-programming throughput is affected by device-handling time; testing, programming, and verification time; and programming yield.

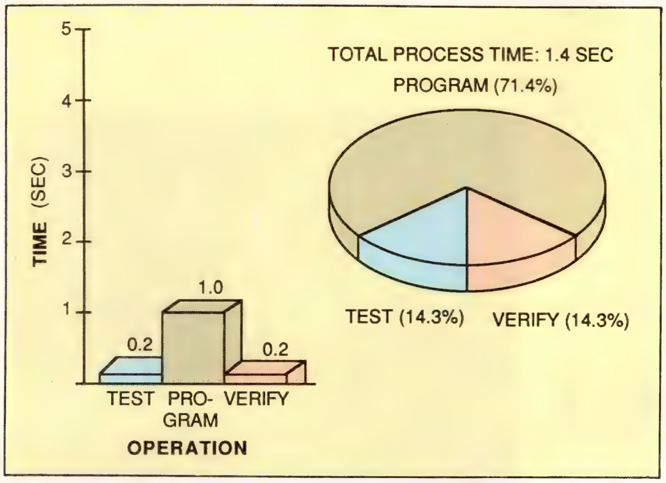

***Fig 6—Optimized programming equipment closes the gap** between a device's theoretical programming time and the programming time you can actually obtain. The Series 1000 programmer specs an overhead of approximately 200 μsec, so it lets you program a 2764 EPROM, which has an 800-μsec programming time, in 1 sec. The programmer also reduces EPROM test and verify times to about 200 μsec each, bringing the time for the total programming process to less than 2 sec.*

technique's per-part programming time is 1.2 sec; the serial technique's programming time is 36 sec per part.

The programming cycle you obtain when you use Intel's Quick-Pulse Programming algorithm (illustrated by the flowchart in **Fig 4**) is much different. **Table 3** gives the programming and handling times for 2764 EPROMs programmed with the parallel and the serial methods, optimized programming equipment, and the Quick-Pulse algorithm. The figures for the parallel mode reveal that although the Quick-Pulse algorithm significantly reduces the EPROM-programming time, the handling time—the time spent inserting the EPROM in and removing it from the programmer—still limits programming throughput. In fact, the serial programming method has a slight edge over the parallel technique. For standard DIP EPROMs with programming times of less than 5 sec, serial programming techniques generally yield the highest throughput.

Reducing EPROM-programming time

The Quick-Pulse programming algorithm allows for shorter programming times because it uses 100-μsec programming pulses. It uses the intelligent algorithm technique, but has no overprogram pulse. The programming time for a 2764 EPROM programmed on a Data I/O Model 120 programmer with the Quick-Pulse algorithm is 10 sec **(Fig 5).**

Although the 10-sec time is an improvement over the programming time you can obtain with the Inteligent algorithm, it's still not optimum. After all, at 100 μsec/byte with no overprogram pulse, the Quick-Pulse algorithm can theoretically program a 2764 EPROM in 800 μsec.

The 9.2-sec difference is caused by the device programmer's operating overhead—the time the programmer needs to manipulate power supplies, address memory locations, perform general houskeeping chores, and so on. (You can generally find a device programmer's operating overhead among the programmer's other specifications; manufacturers usually refer to it as "programming time.")

To take advantage of the short programming times possible with the Quick-Pulse algorithm, therefore, you need to use a device programmer that specs very low operating overhead. For example, the operating overhead of the Series 1000 programmer from Data I/O is 200 μsec, which is just a fraction of the programming time **(Fig 6).** The overall programming time for a 2674 EPROM on this programmer, therefore, is 1 sec. The reduction in programmer overhead and programming time leads to a significant increase in programming throughput.

Finally, to take full advantage of the fast algorithm, your programmer must also reduce test and verify times. As **Fig 6** shows, test and verify times for the Series 1000 are each about 200 msec, so the total programming process takes less than 2 sec. **EDN**

Author's biography

Denise Slocombe is a senior product manager at the Programming Systems Div of Data I/O Corp (Redmond, WA), where she is responsible for strategic and tactical marketing of programming systems for production applications. Her tasks include research, product definition, pricing, promotion, and sales distribution. Denise, who has been with the company for three years, holds BA and MS degrees in mathematics from San Jose State University. In her spare time, she enjoys sailing, skiing, reading, and karate.

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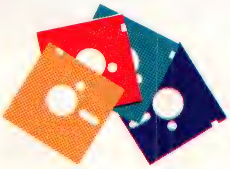

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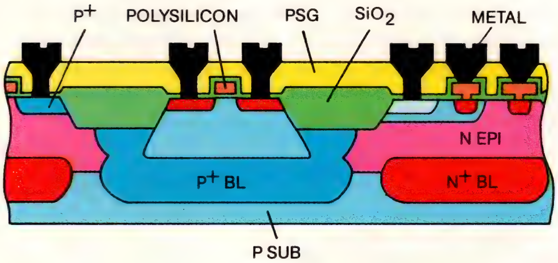

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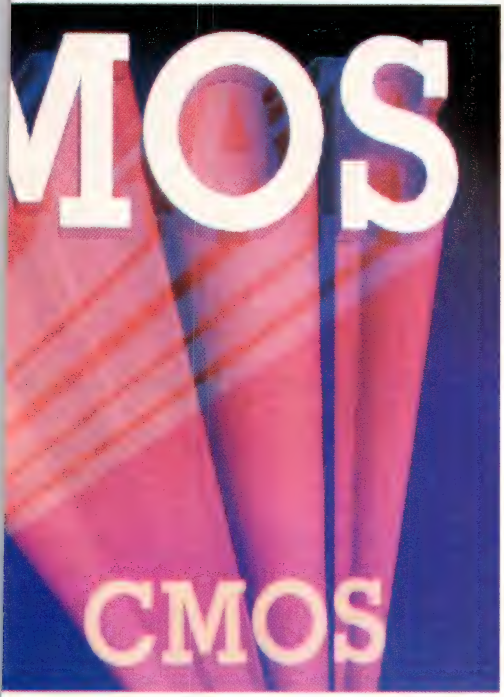

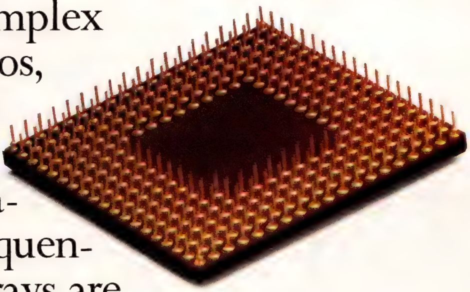

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DESIGN IDEAS

EDITED BY TARLTON FLEMING

Digital window comparator is programmable

Mark T Kraft
Baker Instruments, Allentown, PA

A RAM chip is easily programmable for use as a window comparator on a parallel stream of data. First, store a one in the zero-bit position for all memory locations except those corresponding to the desired range (window) of numbers; store a zero at those zero-bit positions. Next, apply the data stream to the RAM's address port. The RAM's D_0 output will go low for all input words that fall within the window.

Fig 1 extends the window-comparator idea to two 8-bit variables X and Y, which are screened by the 256×4-bit RAMs IC_3 and IC_4. In this case, a microprocessor system examines data representing pulse height (X) and pulse width (Y). The output $\overline{\text{Within Window}}$ goes low only when the D_0 output of each RAM is low, that is, for pulses whose duration and amplitude are both within the ranges of interest.

RAM access time limits the speed of circuit operation. For example, the Am9101 family offers 250- to 1000-nsec access times, and the faster, pin-compatible Am9122 family offers 25- to 60-nsec access. **EDN**

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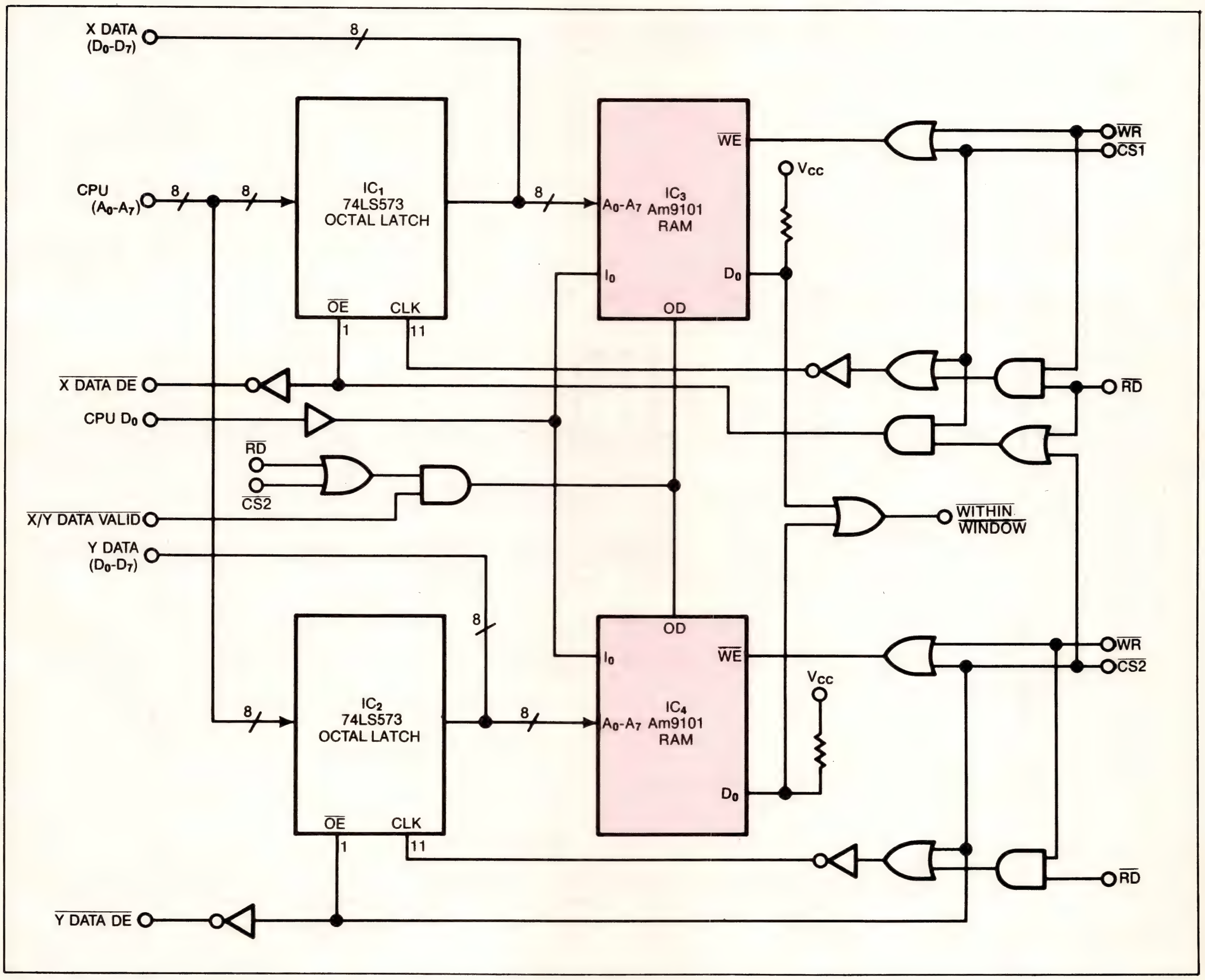

Fig 1—Two RAMs perform window discrimination *on data streams X and Y, producing an output* $\overline{\text{Within Window}}$ *only for word pairs in which each word fits within its respective window.*

Multiplexer limits complement data

S Murugesan
ISRO Satellite Centre, Bangalore, India

Fig 1's circuit reduces the number of bits in a data word without lowering its resolution. For 12-bit, 2's-complement input data D within a given range, the eight output bits D′ are the same as corresponding input bits. For data outside the range, D′ gives a saturated value plus polarity indication.

For input values between −128 and +128, the under/overrange detector's output C is 0, which selects the multiplexers' A inputs. For data outside the range (that is, either D_{11} is 1 and at least one of D_7 through D_{10} is 0, or D_{11} is 0 and at least one of D_7 through D_{10} is 1), the C output is 1, which selects the multiplexer's B inputs. Thus, the output D′ is 01111111 for inputs above 128 or 10000000 for inputs below −128.

You can limit 1's-complement data with this circuit as well. Connect the multiplexers' B inputs to 1 instead of $\overline{D_{11}}$, and derive control C from the logic OR of input bits D_8 through D_{11}. **EDN**

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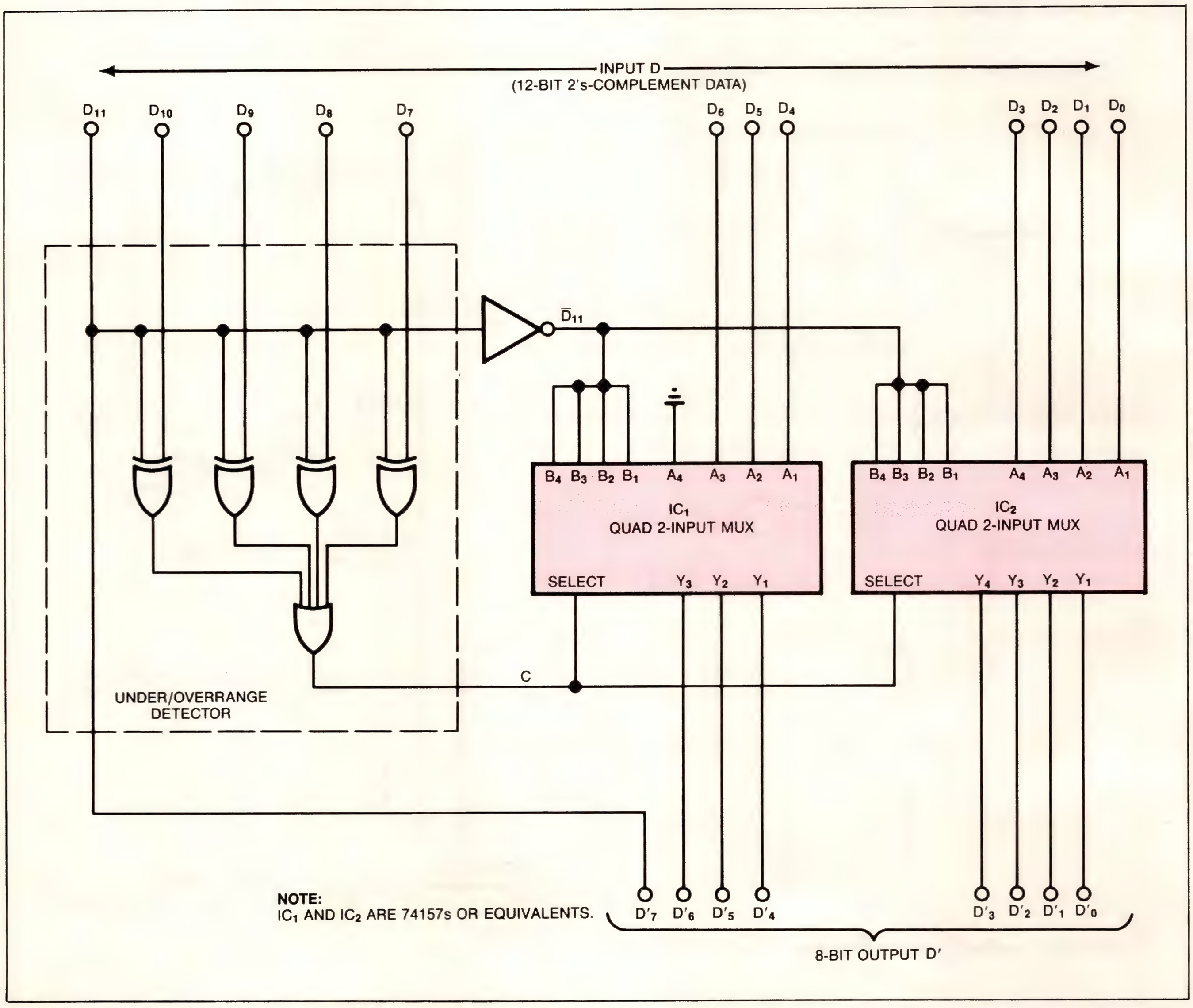

***Fig 1—This circuit converts a 12-bit word to eight bits** without lowering its resolution. Out-of-range data produces a saturated output with polarity indication.*

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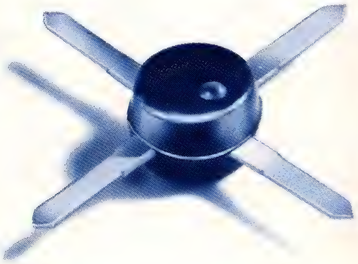

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Photosensors A and B produce quadrature square

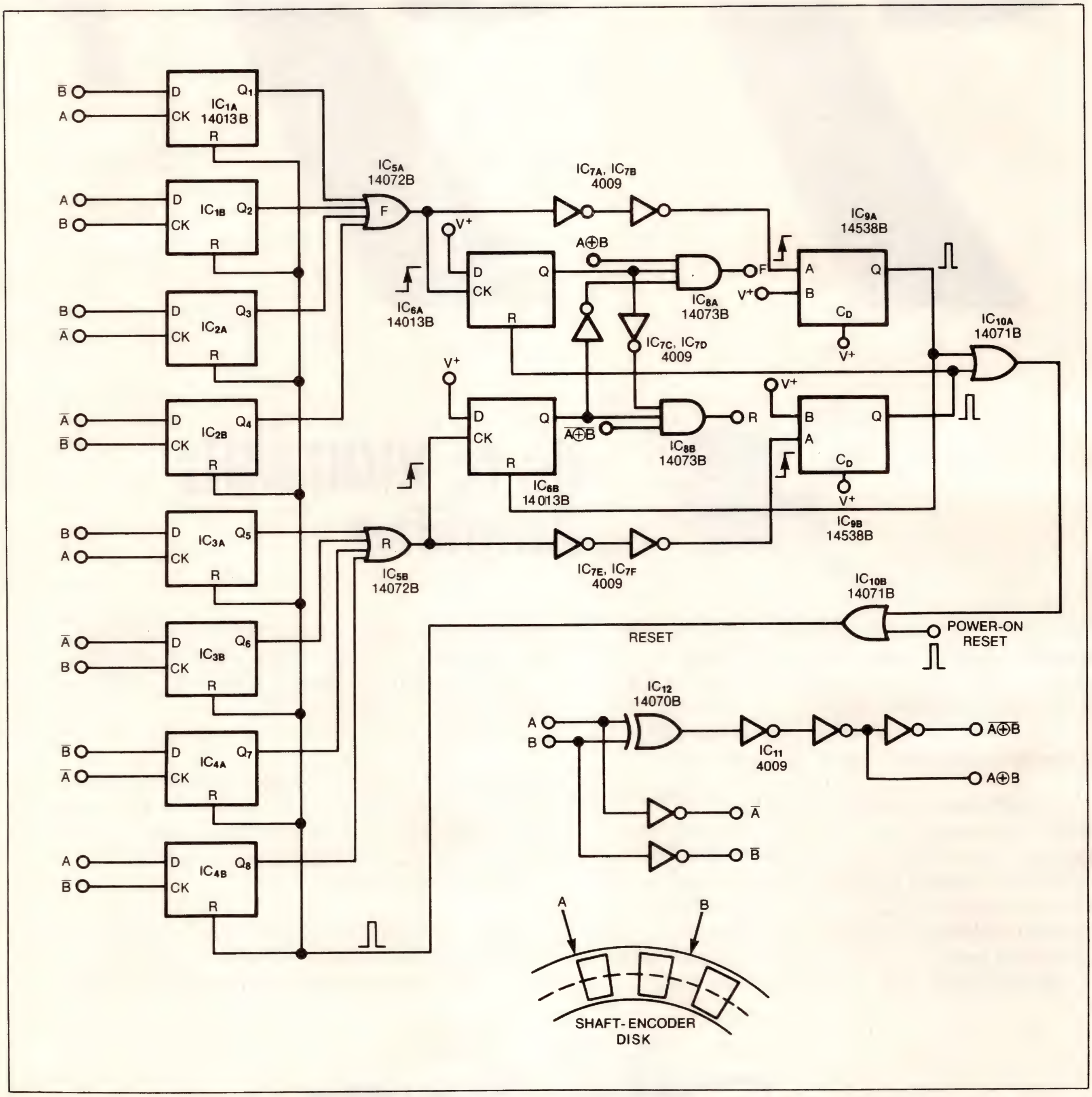
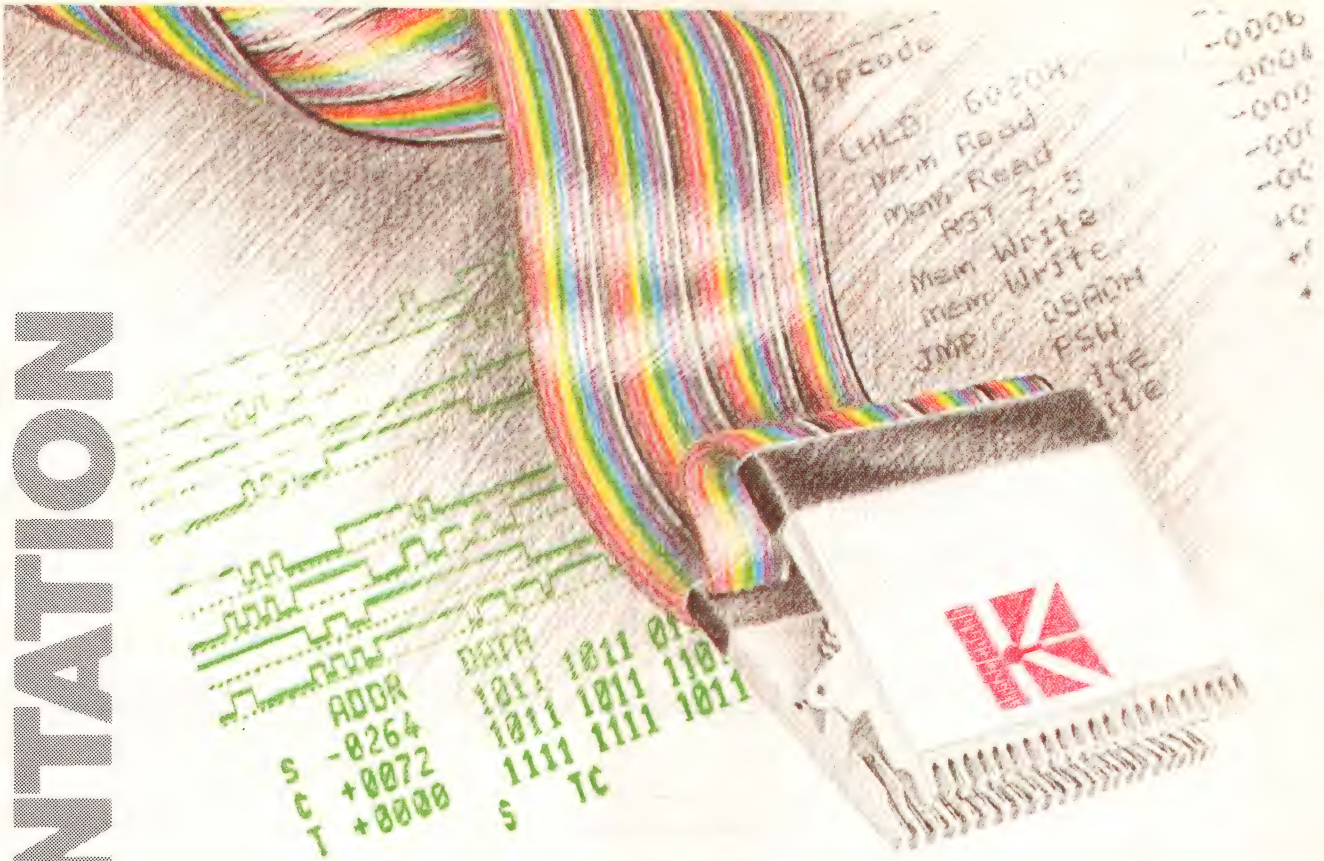


*Fig 1—**This circuit converts** the incremental shaft encoder's photosensor outputs A and B to bidirectional tachometer outputs F (forward) and R (reverse).*

INSTRUMENTATION



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waves **(Fig 2)** as the encoder disk **(Fig 1)** turns. Direction-sense latches IC_1 through IC_4 respond to the eight possible states of A and B, causing the OR gates IC_{5A} and IC_{5B} to identify forward (F) or reverse (R) rotation. The 3-input AND gates IC_{8A} and IC_{8B} provide tachometer pulse-count outputs proportional to the forward or reverse rpm.

IC_9 provides resets to the IC_6 latches. IC_{10} combines these reset pulses to provide a reset to the eight input latches for every change in the state of waveforms A and B, which ensures that the circuit is always ready to detect a change in the direction of rotation. **EDN**

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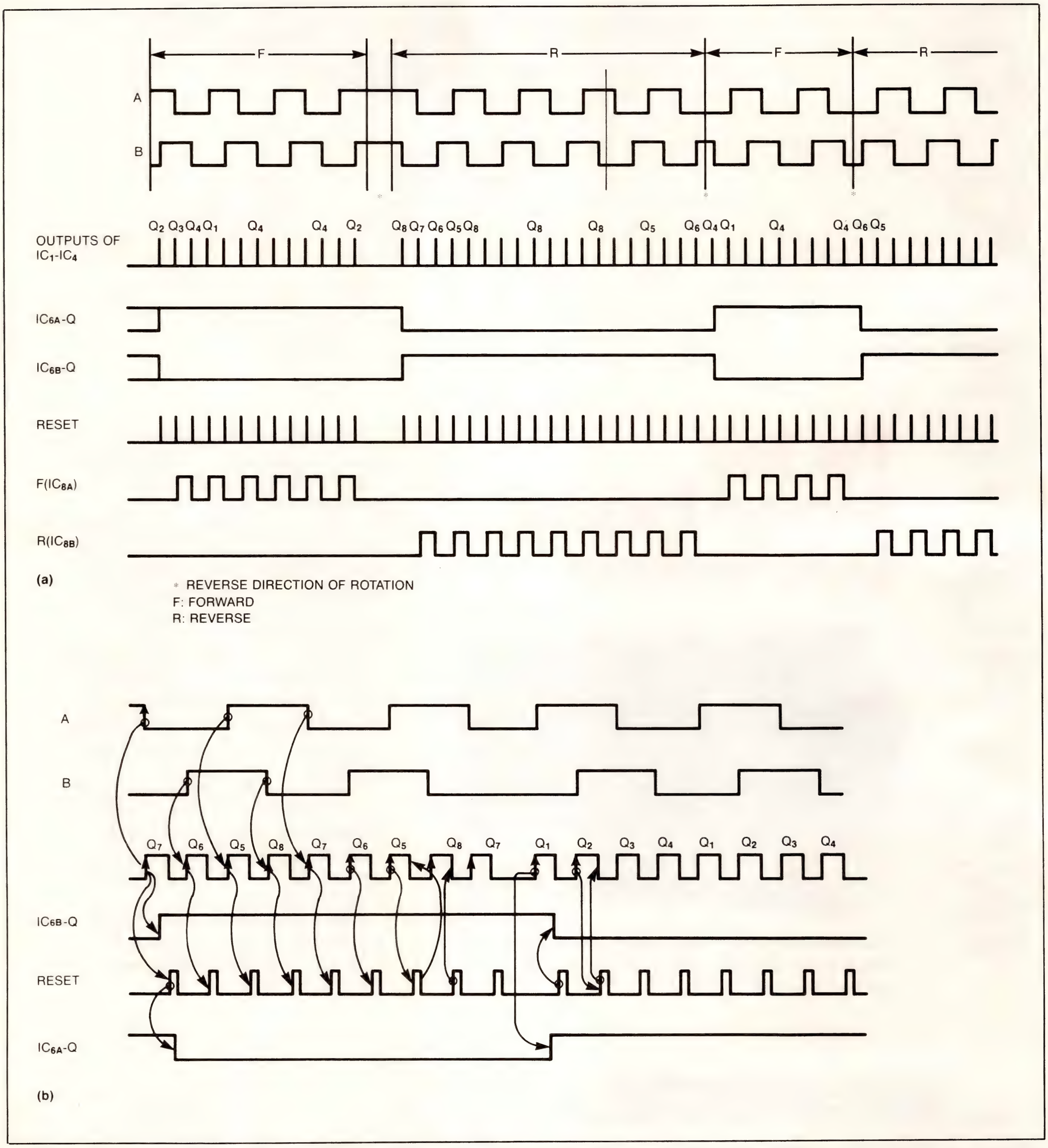
F
R
F
R
A
B
Q2 Q3 Q4 Q1 Q4 Q4 Q2 Q8 Q7 Q6 Q5 Q8 Q8 Q8 Q5 Q6 Q4 Q1 Q4 Q4 Q6 Q5
OUTPUTS OF IC1-IC4
IC6A-Q
IC6B-Q
RESET
F(IC8A)
R(IC8B)
(a)
* REVERSE DIRECTION OF ROTATION
F: FORWARD
R: REVERSE
A
B
Q7 Q6 Q5 Q8 Q7 Q6 Q5 Q8 Q7 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4
IC6B-Q
RESET
IC6A-Q
(b)

Fig 2—These waveforms (a) illustrate the operation of Fig 1. The expanded traces (b) offer greater clarity.

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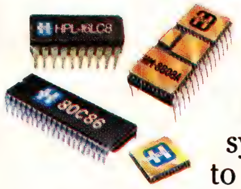

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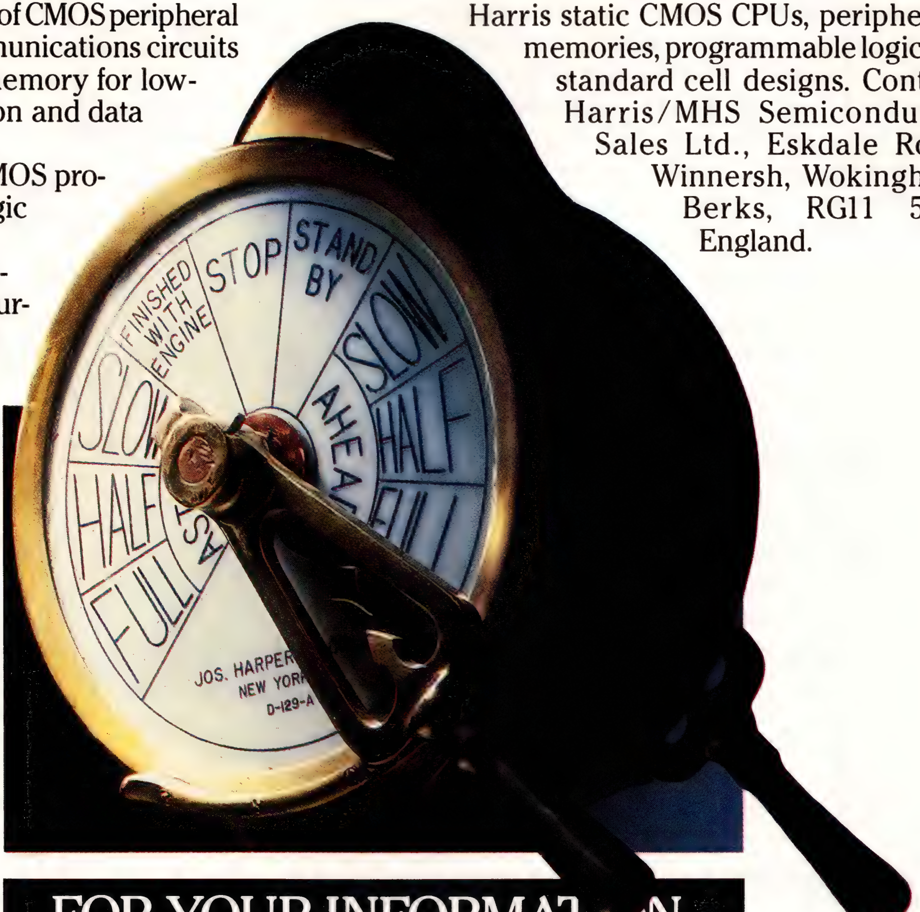

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CIRCLE NO 121

PWM motor controller uses two ICs

Steven Sarns
Vesta Technology Inc, Wheatridge, CO

Fig 1 is a complete, though unconventional, PWM motor controller. In operation, the circuit adjusts the duty cycle of drive signals to the motor until the optical-feedback signal frequency equals the frequency of a VCO in PLL IC_1. The controller can deliver as much as 36V, 3.5A to a motor.

Potentiometer R_1 and the PLL's VCO provide a timebase generator that lets you adjust the pulse rate into comparator II (pin 3) of the PLL. (Comparator I isn't used.) The optical encoder's signal feeds the PLL's Sig input; this reversal of the conventional timebase and signal connections ensures a correct polarity at IC_2's $\overline{\text{Enable}}$ input. A low enable energizes the motor. Pullup resistor R_2 prevents pin 13's high-impedance state from energizing the motor. Switch S_1 lets you reverse the motor's direction.

The controller operates on positive transitions of the PLL's two inputs (pins 3 and 14). Further, it responds quickly because there is no lowpass filter in the feedback circuit. Loading the motor will cause increasing phase lag in the feedback signal, but at 360° the motor is fully on and cannot provide more torque.

This controller provides smooth operation over a 100:1 frequency range for a 30V, ⅛-hp permanent-magnet motor. The number of openings in the encoder disk imposes a lower range limit; the motor's capability to deliver torque imposes an upper limit. **EDN**

To Vote For This Design, Circle No 748

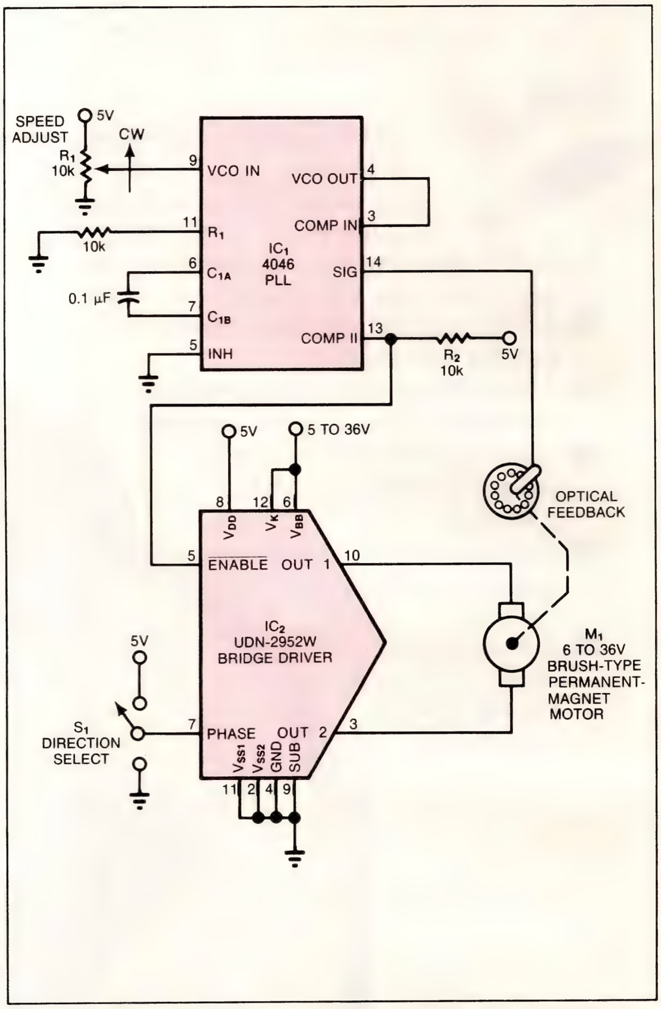


***Fig 1—A PLL and motor-driver chip** provide bidirectional pulse-width-modulated control for a permanent-magnet motor.*

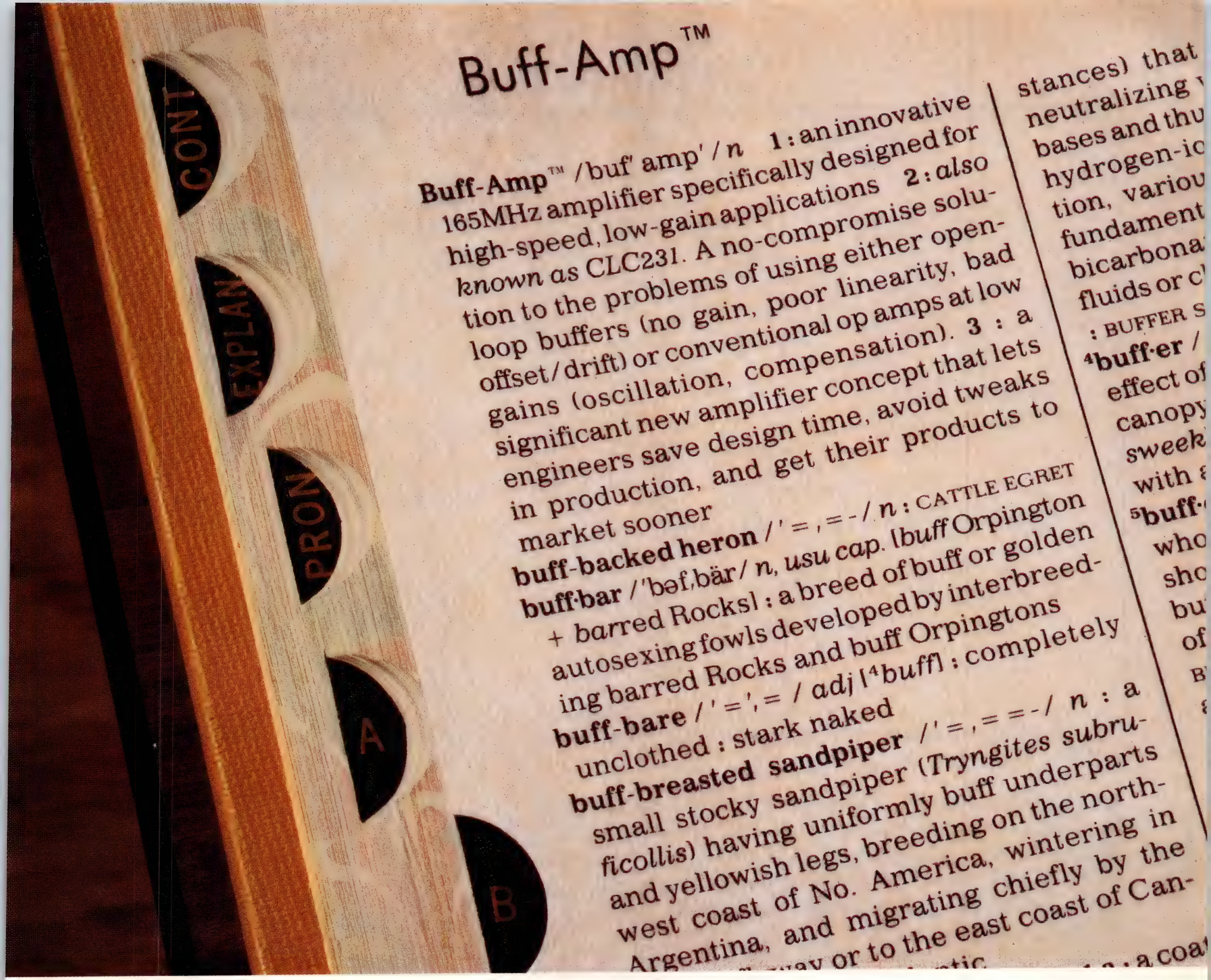
VCO generates frequencies above 40 MHz

Doug Farrar
Apple Computer Inc, Cupertino, CA

The VCO of **Fig 1** is inexpensive, operates from 5V, and generates square, TTL-compatible complementary outputs. In addition, the circuit lends itself to integration because it uses only npn transistors and standard digital functions.

V_{IN} and R_T, along with transistor Q_{1E} and its emitter resistor, set the input current I_T. Current-mirror transistors Q_{1B} and Q_{1D} also each sink I_T. Then, the timing capacitor C_T works with current-source transistors Q_{1A} and Q_{1C} to set the output half-cycle interval. Flip-flop IC_{2B} buffers the heavily loaded Q and $\overline{Q}$ outputs of IC_{2A}.

A high level at IC_{2A}'s Q output, for example, forces Q_{1A}'s base voltage near V_{CC}, which clamps node A about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buff-backed heron /'=,=-/ *n* : CATTLE EGRET

buff·bar /'bəf,bär/ *n, usu cap.* [*buff* Orpington + *barred* Rocks] : a breed of buff or golden autosexing fowls developed by interbreeding barred Rocks and buff Orpingtons

buff-bare /'=',= / *adj* [⁴buff] : completely unclothed : stark naked

buff-breasted sandpiper /'=,==-/ *n* : a small stocky sandpiper (*Tryngites subruficollis*) having uniformly buff underparts and yellowish legs, breeding on the northwest coast of No. America, wintering in Argentina, and migrating chiefly by the

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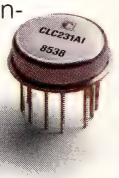

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CIRCLE NO 120

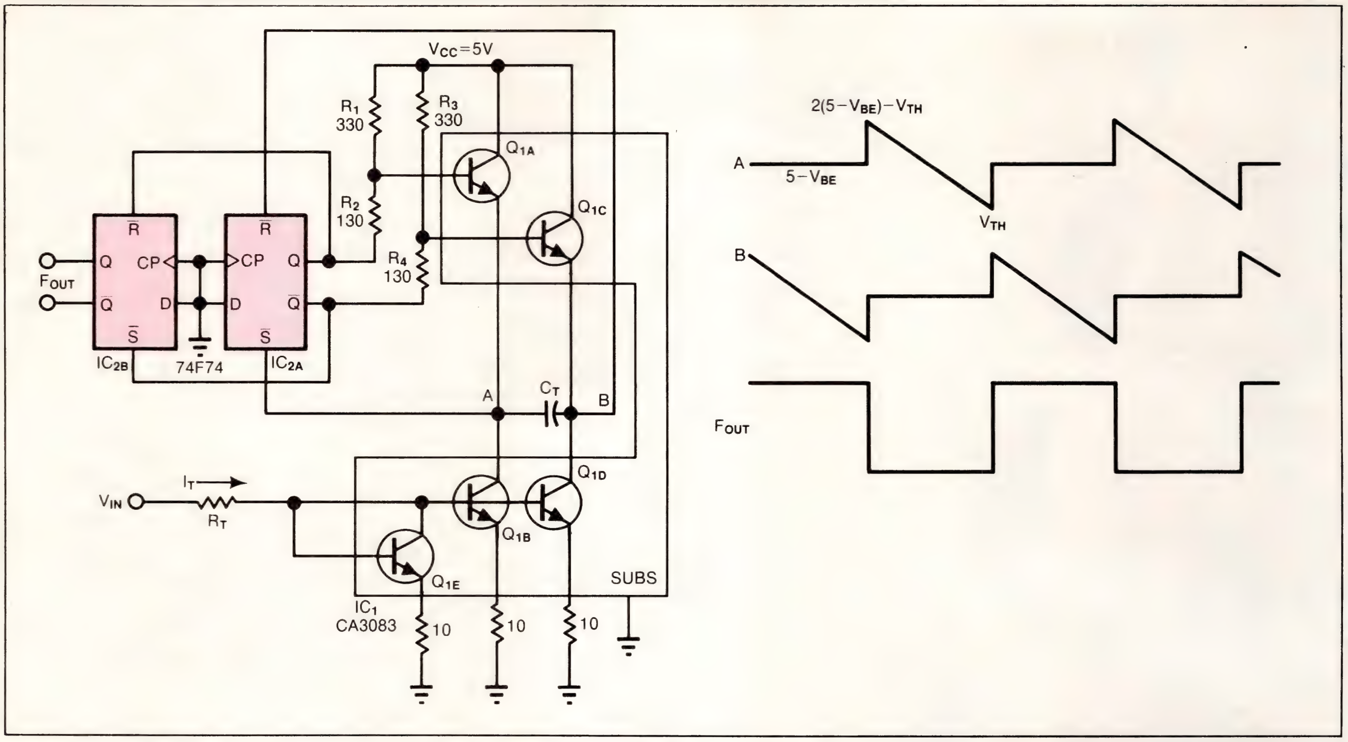

***Fig 1—Two ICs form a voltage-controlled oscillator** that generates TTL-compatible, complementary outputs with maximum frequency above 40 MHz.*

one V_{BE} below V_{CC}. IC_{2A}'s $\overline{Q}$ output is low, so resistors R_3 and R_4 force Q_{1C}'s base to about 1.7V. This action allows node B's voltage to decrease according to a slope determined by I_T and C_T. When B reaches the switching threshold V_{TH} of IC_{2A}'s Reset input (about 1.4V), the flip-flop changes state.

Next, Q_{1C} clamps node B near V_{CC} minus V_{BE}, but the capacitor (charged to $V_{CC}-V_{BE}-V_{TH}$) forces node A to $2(V_{CC}-V_{BE})-V_{TH}$. Because Q_{1A} is back-biased, node A ramps down to the switching threshold of IC_{2A}'s Set input, which toggles the flip-flop again and renews the cycle.

This description of circuit operation applies to timing capacitors greater than 1000 pF. The circuit operates properly for smaller values, but the waveforms are dominated by parasitics; you must use experimental data in place of theoretical predictions of performance. The output waveform remains square, however, for frequencies to 40 MHz and above. **Fig 2** shows measured values of input current I_T vs output frequency for different values of timing capacitance.

Small timing capacitors also allow lower excursions for the waveforms at nodes A and B. Clamps on these nodes ensure that the excursions go low enough to set and reset flip-flop IC_{2A} without saturating the current sources Q_{1B} and Q_{1D}: Resistors R_1-R_4 bias the transistor bases Q_{1A} and Q_{1C} (at 1.7V low) to clamp nodes A and B at about 0.9V min. **EDN**

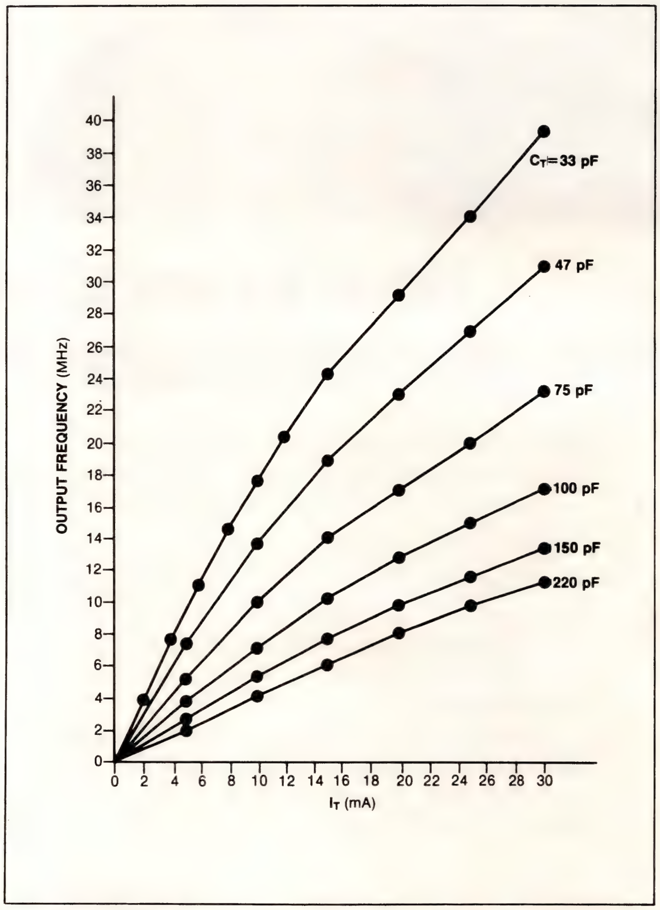

***Fig 2—This graph illustrates** how different values of **Fig 1**'s timing capacitor C_T provide different output frequencies for a given value of input current.*

To Vote For This Design, Circle No 746

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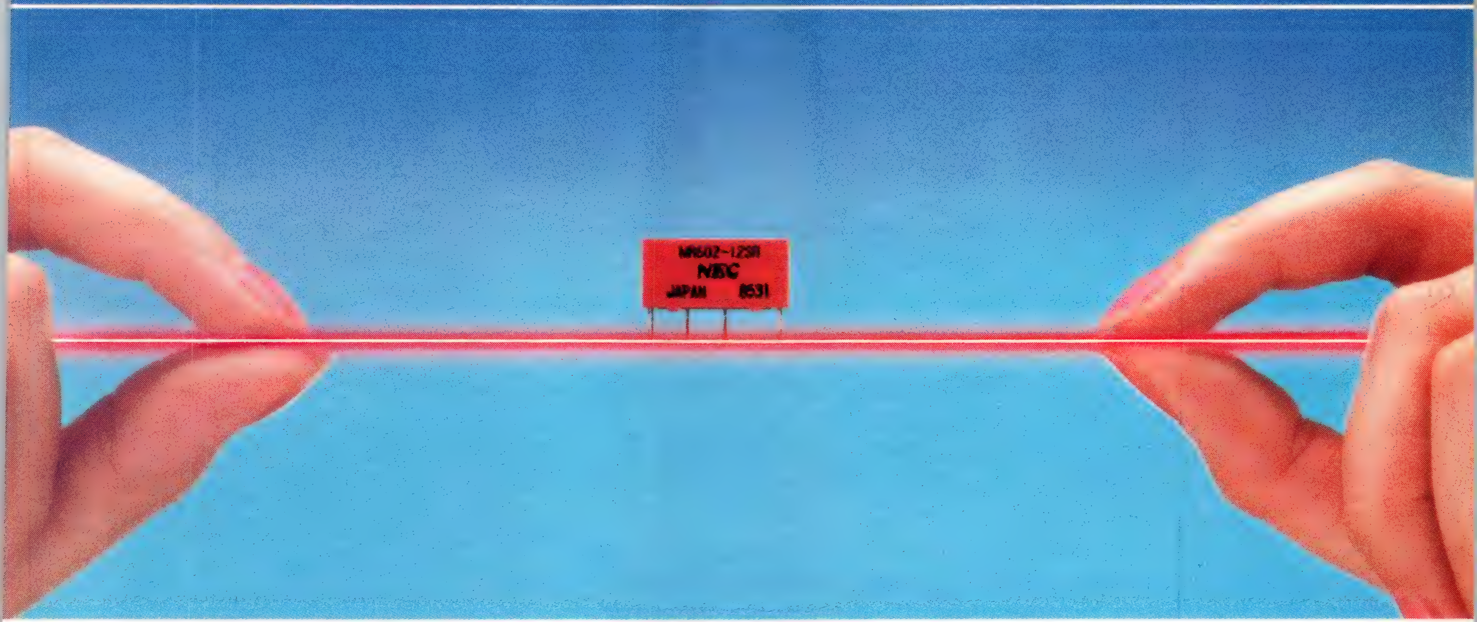

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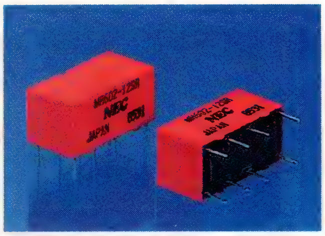

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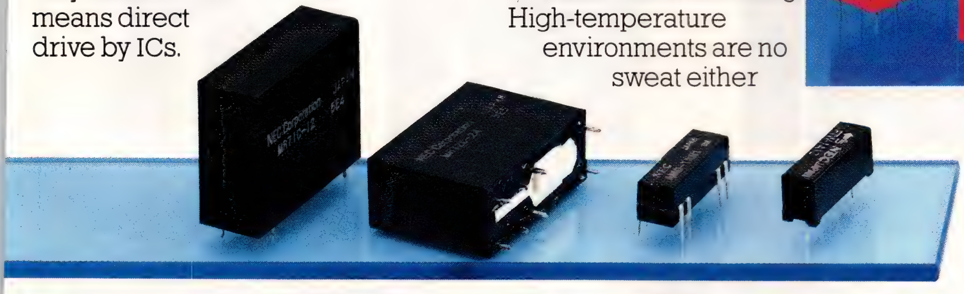

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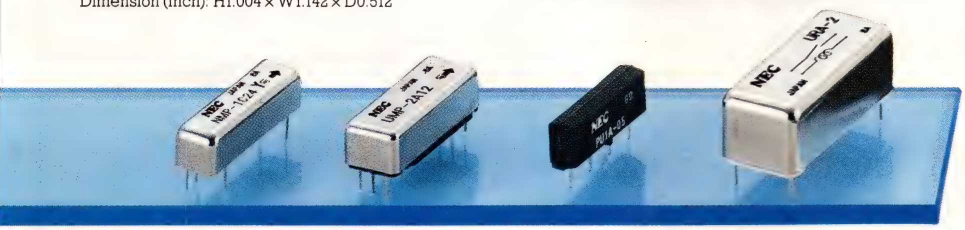

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SIP dry reed relay PU Series.
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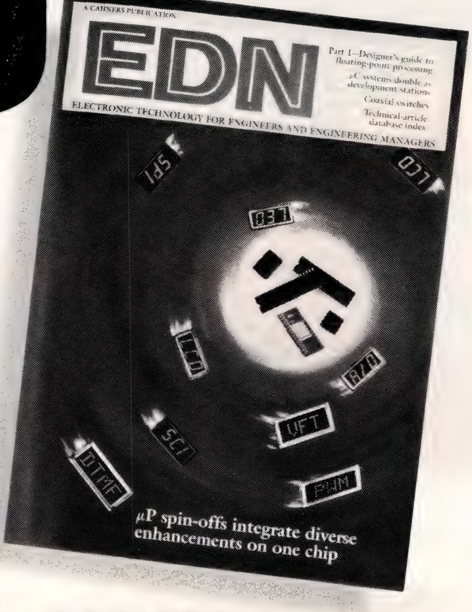
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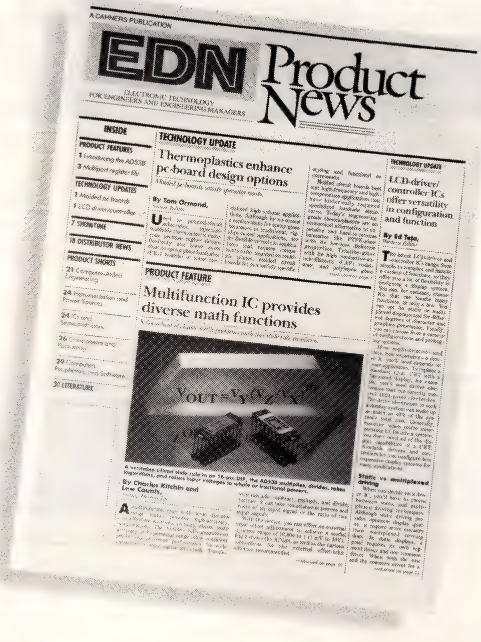
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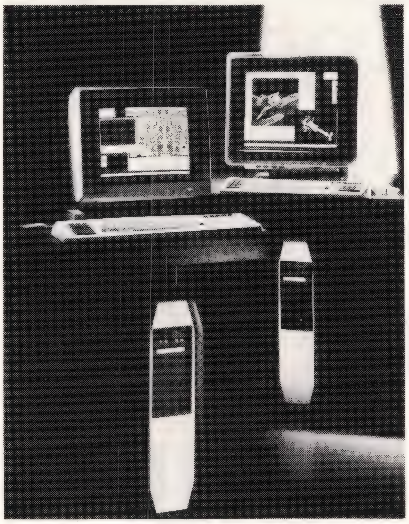

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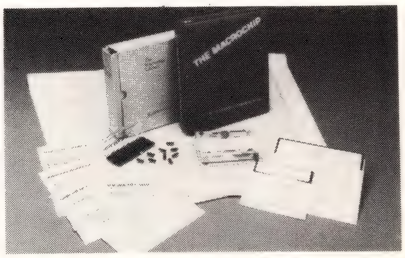

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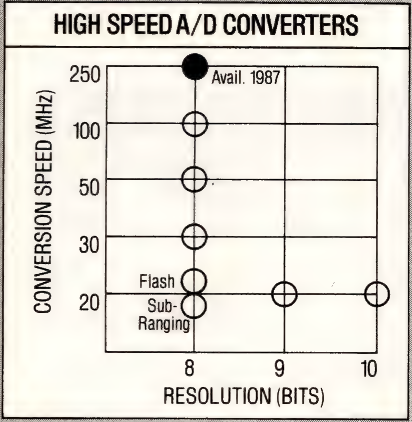
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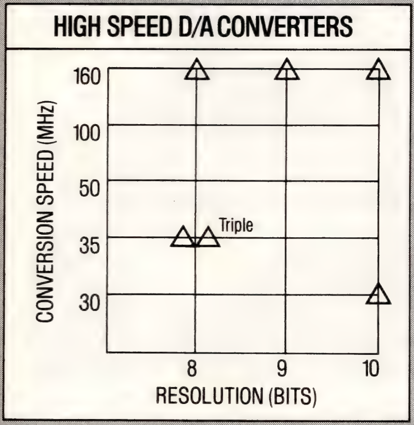
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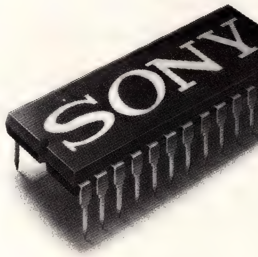

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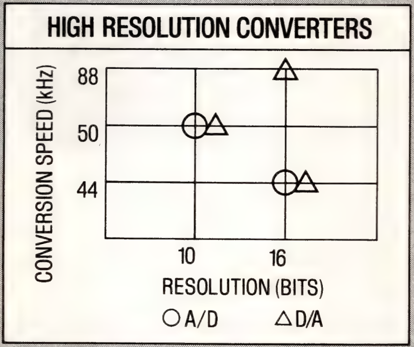
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CIRCLE NO 17

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Ferranti Interdesign, 1500 Green Hills Rd, Scotts Valley, CA 95066. Phone (408) 438-2900.

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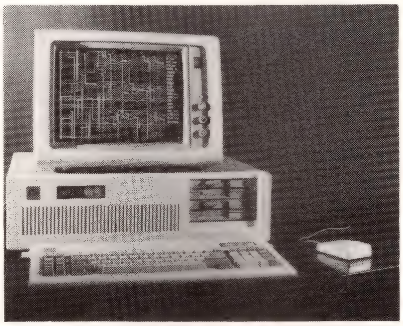

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- *Handles about 3000 equivalent ICs*
- *Combines any of four routing strategies*

Running on AutoCAD, AutoPCD consists of integrated schematic-capture and pc-board-layout packages. The schematic editor lets you partition schematics into hierarchical drawings. Each schematic symbol includes unit and pin numbers, which the schematic postprocessor uses to create a net list and a parts list. A rat's nest utility displays the connection density and wire distribution. The pc-board-layout program can route as many as 3000 equivalent ICs and 32 signal layers. The autorouter provides a choice of four routing strategies: daisy chain, which routes ECL circuits; Steiner, which routes tight layout circuitry; Minspan, which specializes in military boards; and Star, which controls signal-propagation delays and skew tolerances. A prerouter lets you route nets interactively. This pc-board-layout package requires Autodesk's (Sausalito, CA) AutoCAD drafting package. $2500; library options, $395 to $595.

Pro.Lib Inc, 465 S Mathilda Ave, Sunnyvale, CA 94086. Phone (408) 732-1832.

Circle No 354

MICROWAVE DESIGN

- *Produces filter, multiplexer, and impedance-matching networks*
- *Generates files ready to run in Touchstone*

E-Syn version 1.10 synthesizes filter, multiplexer, and impedance-matching networks for microwave or RF design. The package creates a circuit file that can run in Touchstone, the company's program for the design, analysis, and optimization of RF/microwave circuits. In the synthesis program, analysis and optimization are independent of synthesis. Two gradient optimizers ensure convergence. You can design matching networks by using an S-parameter file. The package lets you add inductor-capacitor combinations in series or in parallel. You can transform lumped elements in any analyzed network into distributed

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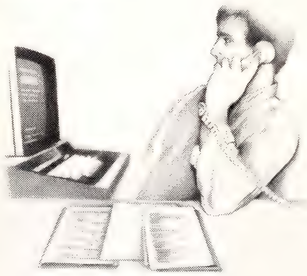

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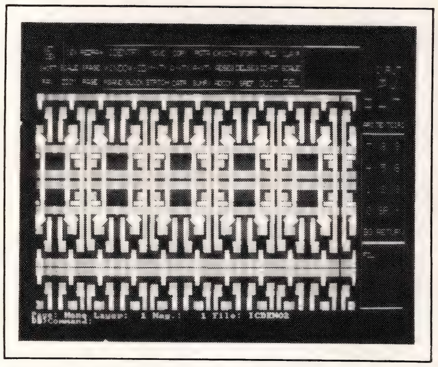
elements. The package runs on the IBM PC/XT and PC/AT, the Hewlett-Packard Vectra PC, and on compatible personal computers that contain 640k bytes of memory, a 10M-byte hard-disk drive, a 360k-byte floppy-disk drive, and a math coprocessor. $5000.

EEsof Inc, 31194 La Baya Dr, Westlake Village, CA 91362. Phone (818) 991-7530. TLX 384809.

Circle No 355



IC-LAYOUT STATION

- *Includes PC/AT and 9-track tape drive*
- *Two-way communication with systems using GDS-II*

The ICD-One workstation lays out custom ICs on a PC/AT and lets you use an IBM PC/AT for 2-way communication with custom-IC layout systems. The IC layout systems must use GDS-II, Calma's (Milpitas, CA) standard IC design-communication format. You can transfer both schematics and cell layouts. The PC-based package provides existing installations with additional IC-design capabilities. The workstation can handle 64k×64k addressable units of design. When you complete each section of a design, you transfer the cells to a larger layout system, such as a Calma GDS II, where you can connect the module to the rest of the chip. The package specs a 0.1-µm resolution. The system includes a 9-track tape drive for direct transfers. You can view only those sets of layers in a design that you are currently using. In this turnkey system, the PC/AT has 640k bytes

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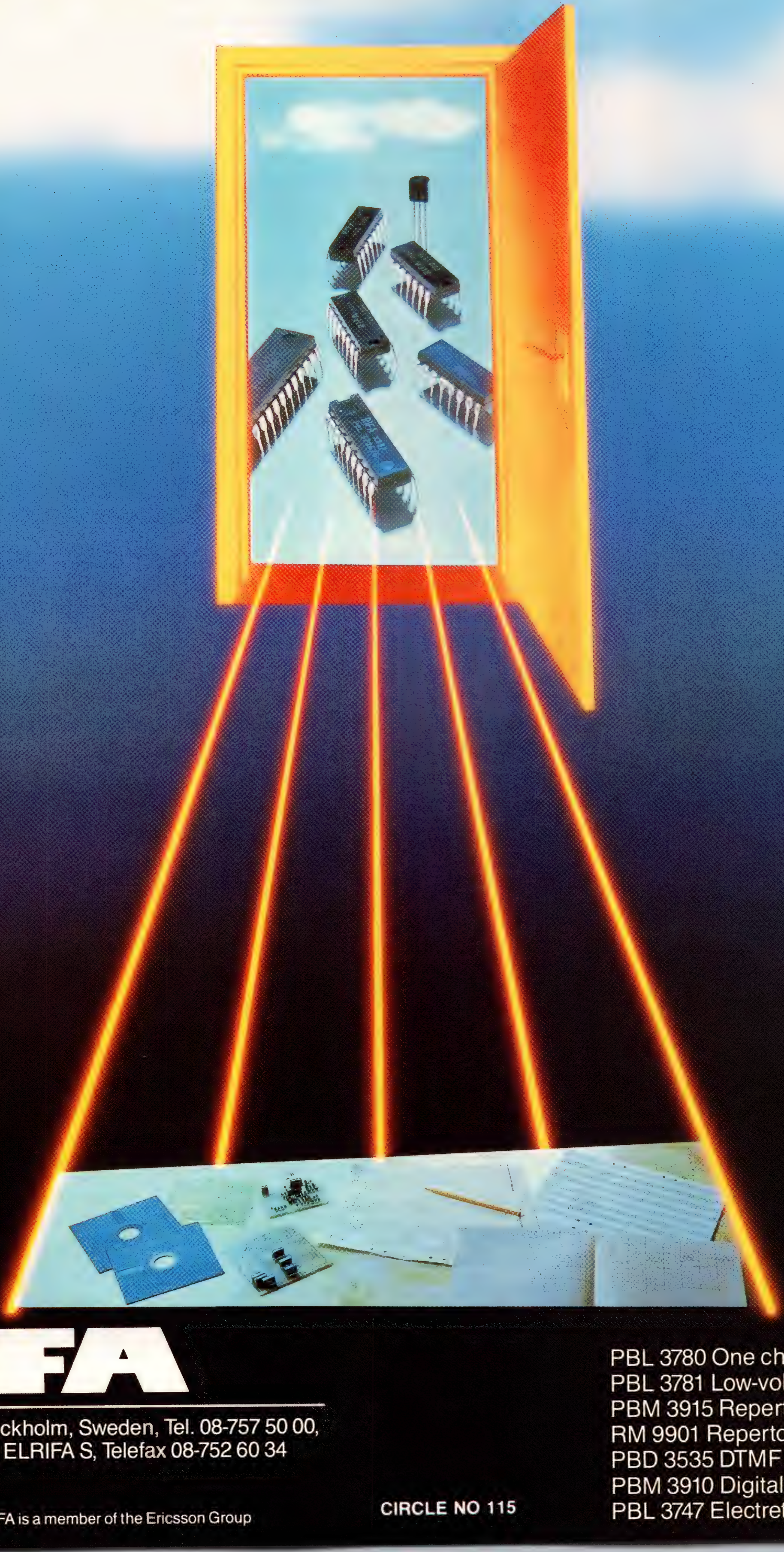

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IFA AB, S-163 81 Stockholm, Sweden, Tel. 08-757 50 00,
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CIRCLE NO 115

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PBL 3781 Low-voltage speech circuit
PBM 3915 Repertory dialler
RM 9901 Repertory pulse dialler
PBD 3535 DTMF generator
PBM 3910 Digital speech controller
PBL 3747 Electret buffer amplifier

IC 1 (86102) A-Ue

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CIRCLE NO 18

of RAM, an 80287 floating-point coprocessor, 1.2M-byte and 360k-byte floppy-disk drives, and a 36M-byte hard-disk drive. The system also includes a color ASCII monitor and a 19-in. 1024×768-pixel color-graphics monitor, an NEC 7220-based graphics controller, and a mouse. $32,000.

Aptos Systems, 4113 Scotts Valley Dr, Scotts Valley, CA 95066. Phone (408) 438-2199.

Circle No 356

CIRCUIT SIMULATOR

- *Spice-based CAE for the IBM PC*
- *Evaluates parameters for Monte Carlo analysis*

Pre_Spice includes syntactical extensions to the Berkeley Spice that let you include libraries, pass parameters to subcircuits, and evaluate tolerance parameters for Monte Carlo analyses. When combined with this company's Is_Spice and Intu_Scope programs, the program provides a complete Spice-based CAE program for the IBM PC. The program is compatible with any version of Spice that conforms to the Berkeley syntax. All three programs, $395; Pre_Spice, $125.

Intusoft, Box 6607, San Pedro, CA 90734. Phone (213) 833-0710.

Circle No 357

LOGIC ACCELERATORS

- *Logic simulation speeds as high as 2M events/sec*
- *Fault simulations at 6M events/sec*

The MX/MXT line of hardware accelerators includes the MX-50, MX-100, MXT-50, MXT-100, and MXT-400. These units offer logic simulation as fast as 2M events/sec and fault simulation as fast as 6M events/sec. The systems are interactive and can handle multiple users. You can interface the hardware accelerators to CAE systems from Mentor and FutureNet. The MXSim software package includes compilation, simulation controls (such as breakpoint, save, and restart commands), and output reports. The systems communicate via a parallel interface with VAX, IBM PC/XT and PC/AT, and Apollo workstations. A hierarchical incremental compiler can compile 10,000 to 20,000 gates in a few minutes on the hardware accelerator. $49,000 to $295,000.

Xcelerated Computer Aided Technology Inc, 1001 S 2nd St, Hopkins, MN 55343. Phone (612) 933-0921.

Circle No 358

TIMING ANALYSIS

- *Calculates device delays*
- *Runs on Scaldsystem and Scaldstar workstations*

The ValidEZlib library-development tool calculates delays automatically. To use the program, you enter a device technology's timing specifications into a template file. The package automatically calculates delays and assigns them to the corresponding device models. For existing models, you need only edit the file; the package then automatically creates new models. This package consists of two programs: Make Template and Make Delay. To create a new library, you use Make Template to make a copy, or template, of an old library (as long as the logical functions are unchanged), and you edit the template by updating timing information. Whether it's creating a new library or editing an existing one, Make Delay extracts information from the template file, calculates appropriate delays, and creates a new library. The package runs on Scaldsystem and Scaldstar workstations. $5000.

Valid Logic Systems Inc, 2820 Orchard Pkwy, San Jose, CA 95134. Phone (408) 945-9400. TLX 3719004.

Circle No 359

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CIRCLE NO 19

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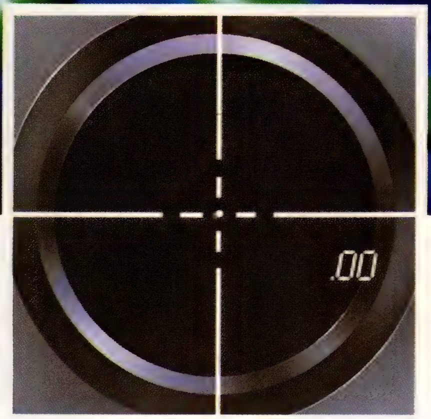

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CIRCLE NO 119

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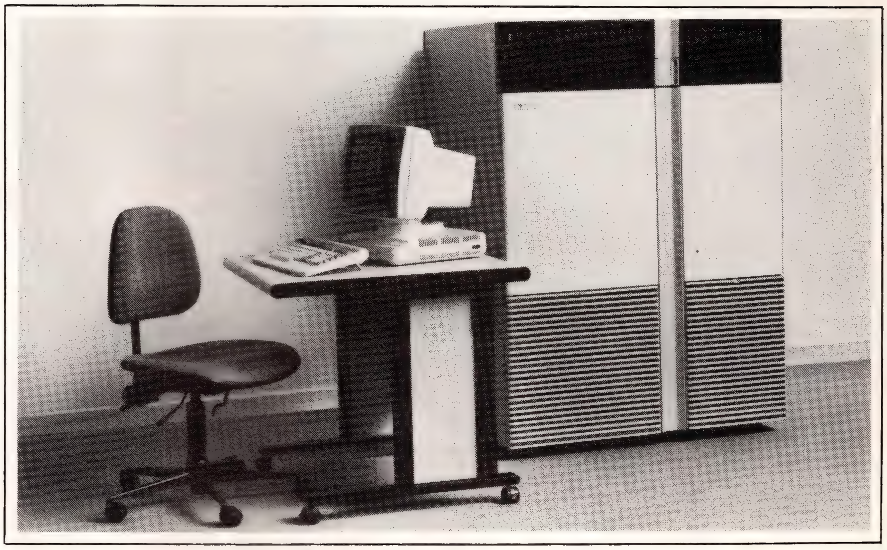
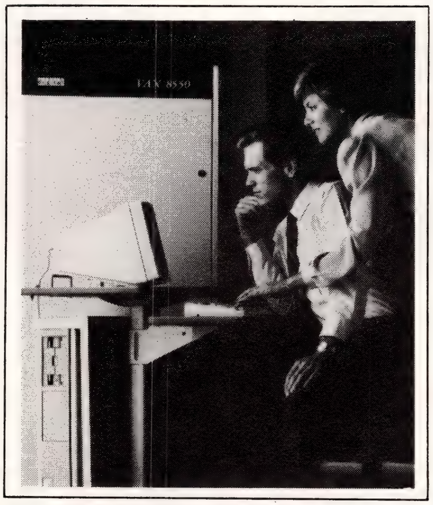


The Nonstop EXT10 and EXT25 computer systems feature fault-tolerant architectures for continuous processing. The EXT10 has dual μPs with 10-sec cycle times and 4M or 8M bytes of memory per μP. The EXT25 reduces the cycle time for its dual μPs to 83.3 nsec and increases the amount of memory per μP to 8M or 16M bytes. The EXT10 accesses one 16-bit word per memory cycle for a transaction throughput of 4 transactions/sec; the EXT25 accesses four 16-bit words per memory cycle and provides 11 transactions/sec. You can expand either system to double its output. The cabinet occupies 8.3 ft^2 of floor space. The standard EXT10 contains two 128M-byte Winchester drives; the standard EXT25, four drives. Both models come with a cartridge tape drive and 15 I/O slots. EXT10, $82,500; EXT25, $325,000.

Tandem Computers Inc, 19191 Vallco Parkway, Cupertino, CA 95014-2599. Phone (408) 725-6000.

Circle No 361



32-BIT COMPUTER

- *Offers six times the power of the VAX-11/780*
- *Occupies 5.6 ft^2 of floor space*

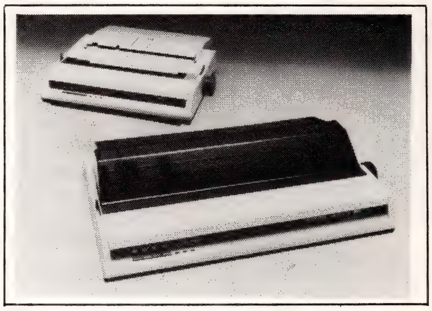
The VAX 8550 can deliver as much as six times the processing power of a VAX-11/780. Its 32-bit μP and 64k-byte cache memory yield a 45-nsec cycle time and facilitate a maximum system I/O rate of more than 16M bytes/sec. A 20M-byte main memory is standard; you can order it with as much as 80M bytes of main memory (the computer offers 4G bytes of virtual-address capacity). The standard VAX instruction set, VMS operating system, and VAXBI bus architecture ensure compatibility with other VAX computers. $394,000.

Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Phone local office.

Circle No 362

200-CPS PRINTERS

- *Print speeds ranging from 40 to 200 cps*
- *Front panel offers menu-selectable print modes*



The 192 Plus and the 193 Plus printers feature 9-pin printheads and let you produce documents in any one of four modes: a 200-cps draft mode, a 160-cps utility mode, an 80-cps emphasized/enhanced mode, or a 40-cps near-letter-quality mode. The 193 Plus features a wide carriage. You select print modes and default settings from menus on the front panels of both printers, which then store your selections in battery-backed memory, thus eliminating DIP-switch manipulation. Other features include semiautomatic sheet feeding, thick-form (0.014-in.) handling, and continuous-form feeding through the top or bottom of the unit. You can order an optional cut-sheet feeder that holds as many as 170 sheets. Both printers are IBM compatible and emulate the

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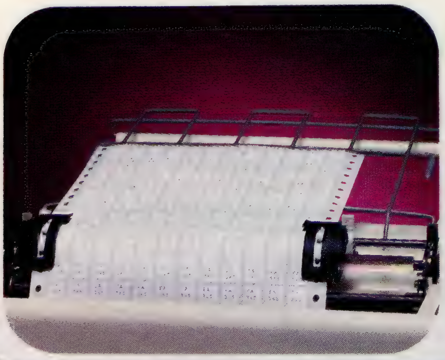

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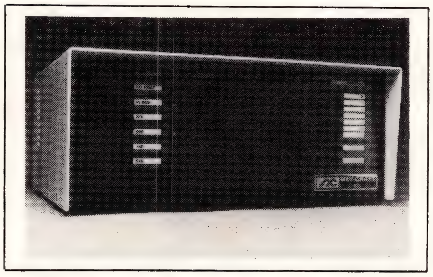
CIRCLE NO 202

IBM 5152 graphics printer and the IBM 4201 Proprinter. 192 Plus, $499; 193 Plus, $749.

Okidata, 532 Fellowship Rd, Mt Laurel, NJ 08054. Phone (609) 235-2600. TWX 710-897-0792.

Circle No 363



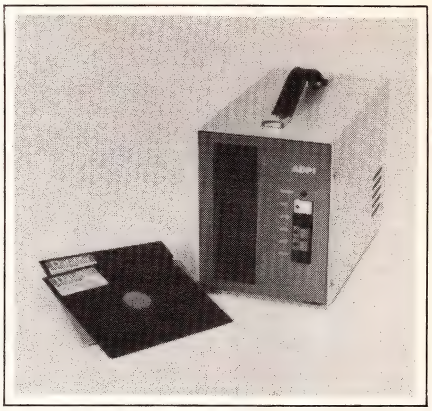
PROTOCOL CONVERTER

- *Menu-driven unit*
- *Two levels of security available*

Allowing you to connect as many as seven ASCII devices to a standard twin-axial port, the 52 Local is a menu-driven protocol converter that provides ASCII terminals with all of the attributes of an IBM 5251 terminal—such as high intensity, reverse video, blinking, column separating, underlining, and embedding of control characters. You can attach ASCII devices directly to the converter, or you can interface the converter to ASCII devices via an asynchronous modem. The unit offers two levels of password security for dial-up users: The device appears to the host computer either as an IBM 5251 Model II terminal or as a 5224, 5225, or 5256 printer. The base unit comes in two versions: Model I is a nonexpandable unit with one RS-232C port; the expandable Model II comes with one RS-232C port and can have as many as seven ports. Model 1, $1295; Model 2, $1450; RS-232C expansion ports, $550.

May-Craft Information Systems Inc, 4312 Beltwood Pkwy S, Dallas, TX 75244. Phone (214) 392-3766.

Circle No 364



DATA TRANSFER

- *RS-232C data-transfer device*
- *Reads and writes 5¼-in. PC-DOS disks*

The Easi-Disk storage and transfer system gives you a portable means of transferring data to and from your IBM PC-compatible computer as well as a way to generate 5¼-in. floppy disks that are PC-DOS compatible. Suitable for performing data dumps from solid-state memo-

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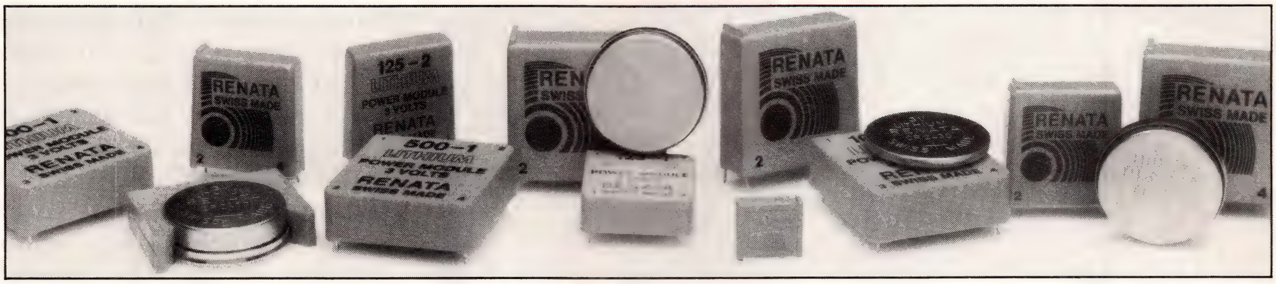

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ry or for acquiring field data from instruments, the system can transfer data via its RS-232C interface at switch-selectable speeds ranging from 110 to 19.2k baud. The unit is controlled by a Z80 μP and has a 360k-byte storage capacity, a 4k-byte addressable RAM buffer, and a 4k-byte PROM control program. $800 (OEM qty).

Analog & Digital Peripherals Inc, 815 Diana Dr, Troy, OH 45373. Phone (513) 339-2241.

Circle No 365

NETWORK ANALYZER

- *Automates network monitoring, testing, and troubleshooting*
- *Handles line speeds to 128k bps*

The Model 600 protocol/performance analyzer automates network monitoring, testing, and troubleshooting and lets you develop additional programs to customize your analysis. The analyzer comes with a 7-in. CRT, two floppy-disk drives that store as much as 1.6M bytes of data, and a proprietary command language for high-level programming. While the unit monitors your network, it gathers statistics on response times and errors, and then graphically displays the data on its CRT. Network analysts can thus observe online network performance without having to interpret raw data. The unit uses multiple 16-bit μPs and a bit-slice processor to perform analysis at speeds reaching 128k bps. $13,995.

Digilog Inc, 1370 Welsh Rd, Montgomeryville, PA 18936. Phone (215) 628-4530.

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CIRCLE NO 157

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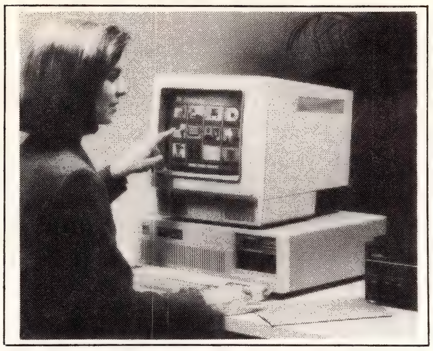
Zax Corporation

CIRCLE NO 167



TOUCH DISPLAY

- *Combines PC and videodisk technology*
- *Interactive presentation system*

This interactive presentation system, the InfoWindow display, provides a touch-sensitive computer display system that combines a PC with videodisk technology. You can program this system to present any combination of computer graphics, full-motion or still video, and high-fidelity audio. The display comprises a voice-synthesis chip, RS-232C and IEEE-488 interfaces, two integrated audio speakers, an 8×11-in. screen with 60 IR-sensitive touch spots, and a terminal that contains its own µP for audio, video, touch, and voice-synthesis control. You can order one or two videodisk players for the system. An enhanced graphics card that is included in the PC can superimpose text and graphics stored in the PC over the video stored on videodisks. $4195; application software is available at prices ranging from $180 to $7200.

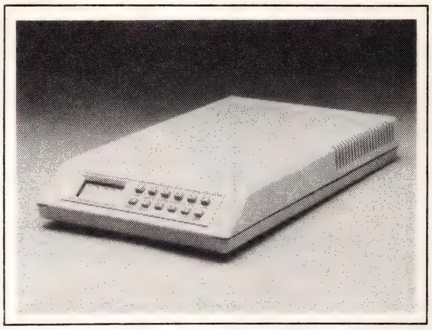
IBM Corp, Information Systems Group, 900 King St, Rye Brook, NY 10573. Phone (914) 934-4828.

Circle No 367

4800-BPS MODEM

- *Supports Bell and CCITT protocols*
- *Includes four autodialers*

Suitable for such applications as remote job-entry batch processing, micro-to-mainframe SNA and bisync data transmission, and database uploads, the 4850PA synchronous modem specs a 4800-bps data-transfer rate. The unit is compatible with both the Bell 208B and the CCITT V.27 communication standards. The 4850PA measures 1½×7×9 in.; its front panel sports an alphanumeric display and keyboard, which facilitate local reconfiguration, number storage, remote



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Now that computers are down on the factory floor, up in airplanes and out in the field, you need solid-state mass storage, like Bubbl-tec® magnetic-bubble memory systems. Unlike disks, they stand up to the dirt, dust, temperature extremes, shock and vibration that plague real-world computing.

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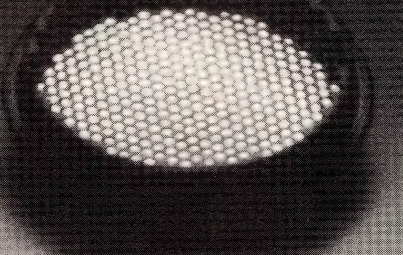
CIRCLE NO 24

What can stop a 650-ton locomotive in its tracks, keep a 7-billion gallon tank from overflowing, and help a blind man cross the street?



This can.

The Polaroid Ultrasonic Ranging System is an accurate, highly sensitive way to detect and measure the presence and distance of objects from 10.8 inches to 35 feet.

It controls industrial robots. And safeguards operators. Measures room dimensions at the press of a button. Warns a truck driver that he's in over his head. And more.

Polaroid introduces a new Environmental Transducer. An improved ultrasonic transducer (available in a sturdy housing) can withstand exposure to a wide range of hostile environments: rain, heat, cold, salt spray, chemicals, shock and vibration. Yet it's just as sensitive as the original transducer used in millions of SX-70 Sonar Autofocus cameras.

Get a $2-million head start on your next product design. Polaroid spent over $2 million developing the Ultrasonic Ranging System. But now you can get this technology in our Designer's Kit for only $165. Or order just the individual components you need for your application.

How far can you take the technology? Call Polaroid's Applications Engineers at 617-577-4681 and find out.

How to get $2-million worth of technology for $165.

To order your Ultrasonic Ranging System Designer's Kit, please send a check or money order for $165 for each kit, plus all applicable state and local taxes, to: Polaroid Corporation, Ultrasonic Components Group, 119 Windsor Street, Cambridge, MA 02139.

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Name

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Company

Address

City State Zip

Polaroid

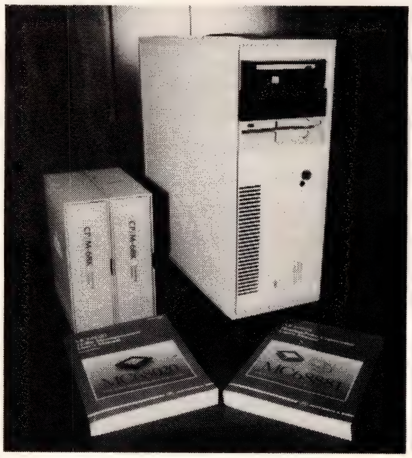
"Polaroid", and "SX-70"®

CIRCLE NO 25

testing, and automatic dialing. The manufacturer also offers a free designer's guide and a sample of the source code, which you can use to integrate the unit's dialing protocols into your communications software. $1295.

Racal-Vadic, 1525 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 946-2227.

Circle No 368



32-BIT COMPUTER

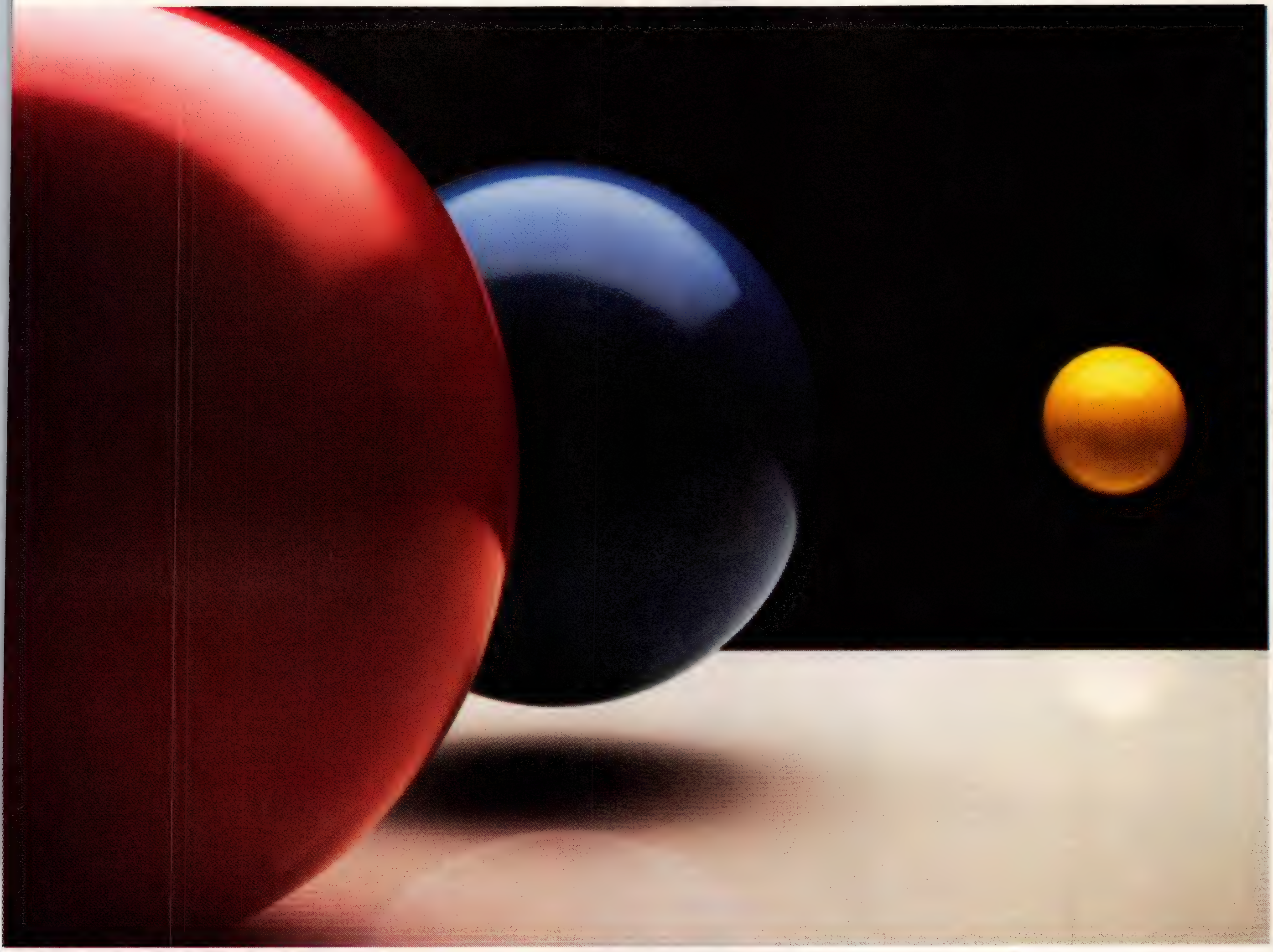
- *Uses a 16-MHz 68020 CPU*
- *Performs 4 MIPS*

The Computerist MainFrame (CMF) is a 32-bit computer that can process as many as 4 MIPS. Its standard configuration includes a 16-MHz 68020 CPU with a DMA controller, 1M byte of RAM, the CP/M-68k operating system, C, a real-time clock with two interval timers, a time-of-day clock, 2k bytes of static RAM, two RS-232C ports, one printer interface, a 369k-byte floppy-disk drive, and a SCSI interface. You can expand the RAM to 113M bytes. The computer is housed in a transportable, rack-mountable enclosure that can hold as many as eight boards and three half-height disk drives. $2500 (OEM qty).

Digital Electronic Systems, 302 S Main, Estill Springs, TN 37330. Phone (615) 649-5137.

Circle No 369

Reach out for good ideas



Good ideas come in smaller case sizes from the capacitor choice.

Nothing moves a product to market faster than timely good ideas.

That's why some of our biggest good ideas in capacitors now come in smaller packages. Features that can offer you new opportunities for improving designs, controlling costs and automatically inserting more high CV capacitors than ever before.

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One good idea after another.

CIRCLE NO 166

Circuit-Board-Artwork Software: $895. And guaranteed.

smARTWORK® lets the design engineer create and revise printed-circuit-board artwork on the IBM Personal Computer. You keep complete control over your circuit-board artwork — from start to finish.

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☐ Multicolor or black-and-white display

System Requirements:

☐ IBM Personal Computer, XT, or AT with 320K RAM, 2 disk drives, and DOS Version 2.0 or later
☐ IBM Color/Graphics Adapter with RGB color or black-and-white monitor
☐ IBM Graphics Printer or Epson FX/MX/RX series dot-matrix printer
☐ Houston Instrument DMP-41 pen-and-ink plotter
☐ Microsoft Mouse (optional)

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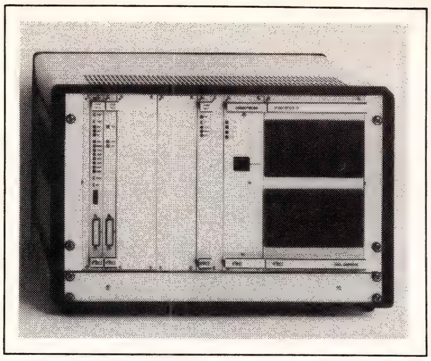
CIRCLE NO 203



VME COMPUTER

- *Processes 3.5 MIPS*
- *Provides a 32-bit, real-time, multiuser development system*

Running at 16.7 MHz with no wait states for 3.5-MIPS performance, the 2P21 VME Bus-based computer provides you with a 32-bit, real-time, multiuser hardware and software development system. The unit contains a 68020 CPU and a 68881 floating-point coprocessor. A standard configuration includes 512k bytes of static RAM, a 51M-byte Winchester drive, a 1M-byte floppy-disk drive, two RS-232C ports, six VME Bus expansion slots, and a 19-in. chassis. You also get a real-time multitasking/multiuser operating system called PDOS, a CRT editor, and a 68000 macroassembler. The PDOS operating system executes 1.8 times faster on the 16.7-MHz 68020 than on a 16-MHz 68000 CPU. Fortran-77, Pascal, and C are available as options. Standard configuration, $15,990.

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (800) 237-8863; in CA, (800) 237-8862.

Circle No 399

KEYBOARD

- *Automatically adjusts for IBM PC/XT or PC/AT*
- *Has separate function and numeric keys*

The KM-5170 keyboard automatically configures itself for the IBM PC/XT or PC/AT. Designed to meet DIN standards, the keyboard has 84 sculptured keys. Function keys such as Enter, Shift, and Control have larger tops. The Cap Lock, Num Lock, and Scroll Lock keys have LED indicators. The keyboard features a separate numeric keyboard and 10 function keys. It measures 30 mm from the base of the enclosure to the top surface of home row. The unit weighs 3 lbs and has retractable feet. $119.

Quimax Systems Inc, 844 Del Rey Ave, Sunnyvale CA 94086. Phone (408) 773-8282.

Circle No 400

LASER PRINTER

- *Generates 24 pages/minute*
- *Emulates the Diablo 630*

The PS 2400 laser printer operates at a speed of 24 pages/minute. Using PostScript as its resident page description language, the PS 2400 can rotate and scale type styles and create line art and halftones with 300×300-dot/in. resolution. The printer comes with 3M bytes of memory and emulates the Diablo 630. It has 13 resident type faces and a symbols font. Face-down paper collation is a standard feature. Available interfaces include RS-232C, RS-422, Centronics parallel, and Appletalk. The unit holds 2000 sheets of 16- to 24-lb letter, legal, or 11×17-in. paper. $29,995.

QMS Inc, Box 81250, Mobile, AL 36689. Phone (205) 633-4300.

Circle No 401

WORLD'S SMALLEST DIP SWITCH

SAME SIZE AS AN IC

BETTER HEAT CONVECTION.

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THE LOW PROFILE K40 DIP IS THE SAME SIZE AS AN IC

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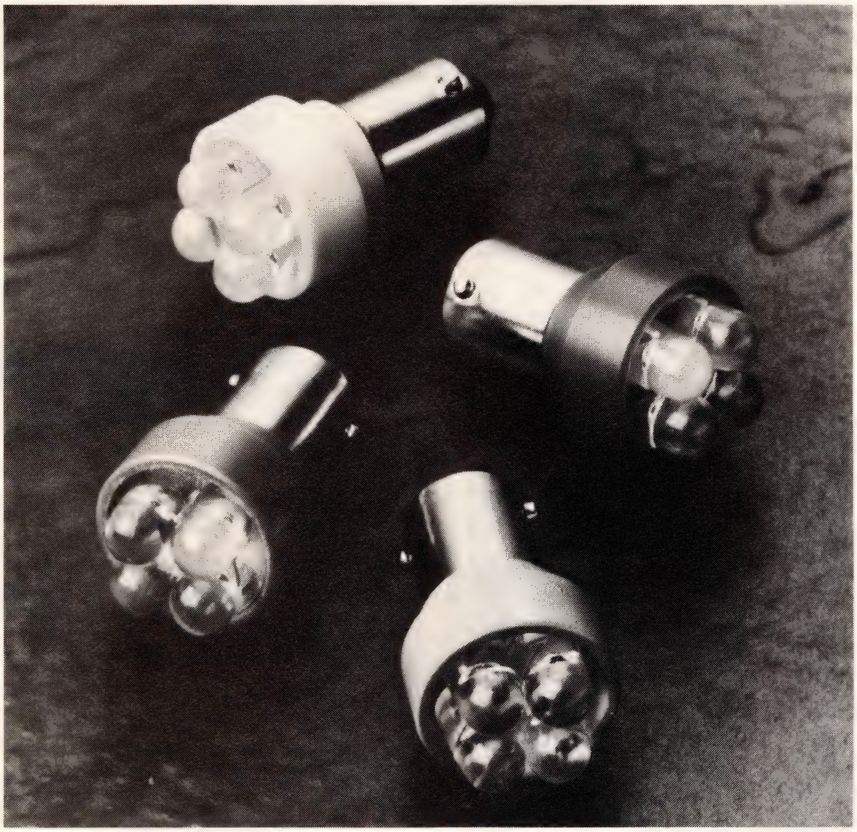
America can do it better!

CIRCLE NO 26

COMPONENTS & PACKAGING



LED ILLUMINATORS

- *Output to 25 cd*
- *Bases are compatible with those of incandescent lamps*

MX400 Series LED illuminators are brighter than the equivalent-sized incandescent lamps and have bases that are compatible with those lamps. The light output can reach 25 cd. A standard configuration and a wide-angle version are available. The standard configuration includes four T-1¾ LEDs mounted in a T-3¼ base. In the wide-angle model, four T-1 LEDs are mounted on the same base; these smaller LEDs generate a total output of 2 cd. You can order various T-3¼ bases, including bayonet, screw, and flange. Because resistors are built into the units, you can select voltage ranges from 6 to 110V ac at a drive current of about 20 mA. The LEDs come in four colors: red, amber, yellow, and green. Because clear lenses are used for maximum light output, the cases are color-coded. $4.50 (100). Delivery, five to seven weeks ARO.

Data Display Products, 301 Coral Circle, El Segundo, CA 90245. Phone (800) 421-6815; in CA, (213) 640-0442.

Circle No 370

D/A CONVERTER

- *12-bit hybrid*
- *Settling times of 110 and 120 nsec max*

The HDM-1210 is a current-output, 12-bit hybrid DAC that features a maximum digital settling time of 110 nsec (to ±0.1%), a maximum analog settling time of 120 nsec (to ±1% FS), and an analog bandwidth of 10 MHz. It can operate with unipolar or bipolar inputs and can perform 1-quadrant multiplication. Two-quadrant and 4-quadrant multiplication is possible if you use two of the converters. The -1210 features guaranteed monotonicity over the operating range and a maximum gain error of ±0.5% FS. Guaranteed differential and integral linearity over the operating range is ±1 LSB. Three versions are available in 24-pin ceramic or metal DIPs for operation over one of two temperature ranges. The BD grade guarantees operation from −25 to +85°C; the SD and SDB grades guarantee operation from −55 to +100°C. BD grade, from $144 (100).

Analog Devices Inc, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (919) 668-9511.

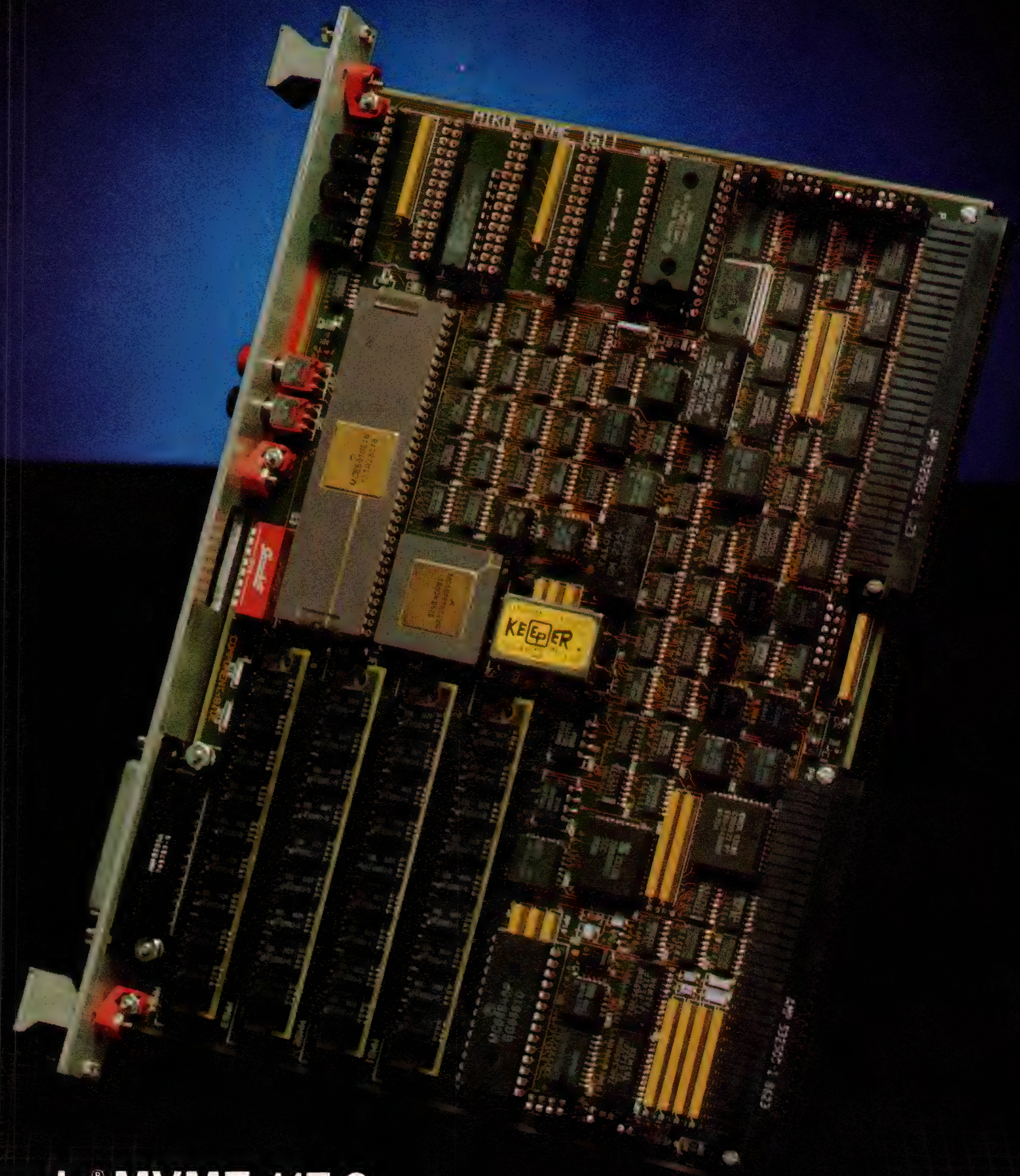
Circle No 371

FIBER-OPTIC MODEM

- *Improves data transmission for IBM 5251*
- *Operates over distances to 5000 ft*

The HFM5300 fiber-optic modem improves the integrity of data transmission for the IBM 5251 and compatible cluster controllers. It plugs directly into the controller without modification. The unit measures 5.25×2.63×1.75 in. It can use fiber-optic cable with a core diameter of 50-, 62.5-, 85-, or 100-μm and handles communication links to distances of 5000 ft. (The IBM 5251 controller's round-trip propagation-delay restrictions limit the distance to that length.) You can use the modem in any of eight positions designed for the 5251 protocol. The device consists of an 850-nm LED transmitter and a detector module.

A Surface Mount Performance
Breakthrough!



A Motorola® MVME 117-3
Compatible CPU Board For Under $1,000!*

The **mikul**® TVME-1611 is a direct plug-in replacement for the MVME-117-3 featuring the latest in surface mount technology plus . . .

- 512K of memory, expandable to 1 megabyte
- Two 8 bit parallel and one serial port
- SCSI interface
- Battery backed-up clock
- Four EPROM sockets for up to 256K of EPROM
- AVAILABLE FROM STOCK

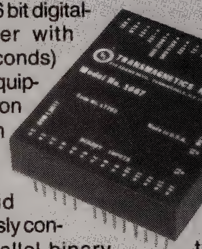
mikul®
A Division of TL Industries
2541 Tracy Road
Toledo, Ohio 43619
419/666-8144

* In quantities of 100 units or more. Pricing in U.S. dollars for U.S. delivery only.

CIRCLE NO 175

CONVERTERS: 16 BIT
DIGITAL-TO-SYNCHRO/RESOLVER

- **0.008° Accuracy**
- **Associated Circuitry for MULTIBUS, VME BUS, STD BUS AND IEEE-488 BUS**



Model 1667 is a 16 bit digital-to-synchro/resolver with 0.008° (30 arc seconds) accuracy for test equipment, high resolution feedback system and similar applications.

This new solid state unit continuously converts a 16 bit parallel binary coded angle into a 3-wire synchro or 4-wire resolver output. It can be supplied with associated circuitry to interface with either the Intel 8085/8086 or IEEE-488 bus.

Transformer isolated design with short-circuit proof 1.3 VA output for frequencies from 50 to 2045 Hz. Any specific voltage output can be supplied. Maximum magnitude variation is 0.03%, and there is no requirement for protection against static electricity. Temperature ranges: 0° to 70°C or -55° to 85°C.

Available hermetically sealed or in hi-rel 883B or MIL-M-38510 designs. Meets MIL-STD-202D methods 101C, 105B, 106C, 202D, 204B and 205D. Requires no calibration, adjustment or warmup.

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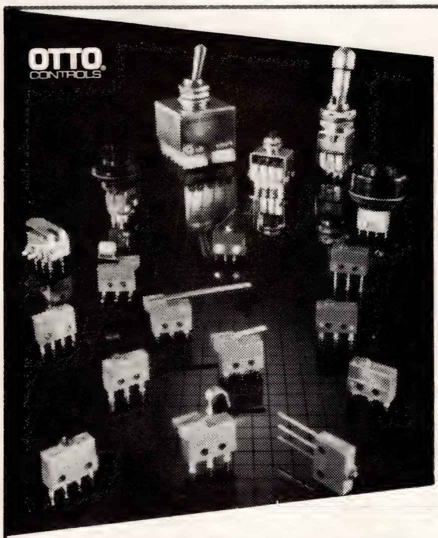
PHONE NO. 516 293-3100 TWX510-224-6420

YOUR DATA CONVERSION HEADQUARTERS.

CIRCLE NO 27

OTTO CONTROLS



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One stop design shopping is yours with OTTO'S complete line of single and double break snap-action switches. Sub-subminiature sizes for direct actuation and for integral or auxiliary lever, pushbutton and toggle actuators. Ratings from 8 amps to low level. OTTO'S patented high contact pressure design assures <0.025 ohms contact resistance. If you don't see what you need as a standard, we'll customize a design for you. Commercial grades are UL listed and CSA certified. Military grades meet MIL-S-8805/4, /76, /101, /106 & /109.

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CIRCLE NO 28

Power Your Communications. Communicate Your Power. With TDK Ferrite Cores.

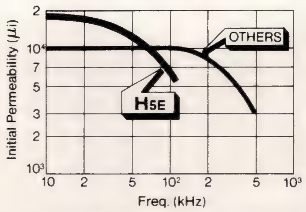
As telecom technology switches to digital, and power supplies switch to switchers, quality and features of ferrite cores take on added importance while generating new reasons to talk to the undisputed leaders, TDK.

Next time you're in our neighborhood, come and take a look at the world's largest production of ferrite materials. TDK manufactures ferrite cores from the raw materials on up, with totally automated production systems. 50 years of experience and a continuous R & D program are reflected in unique features and unsurpassed quality levels.

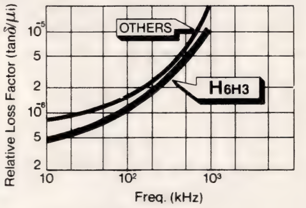
For telecom and power supply applications, TDK ferrite cores include:

- High permeability types such as our H5E
- Low loss types with significantly reduced loss factors up into the MHz range;
- Extremely low power loss and reduced temperature surge types (H7C4);
- TDK original cores, EEC, EP, LP and PQ as well as IEC standard core shapes including EEC, POT, RM, etc.

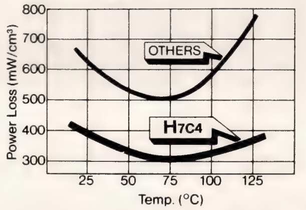
μi vs. Frequency Characteristics

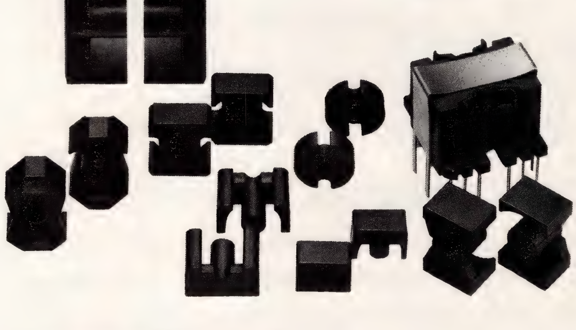


tanδ/μi vs. Frequency Characteristics



Power Loss vs. Temp.





TDK®

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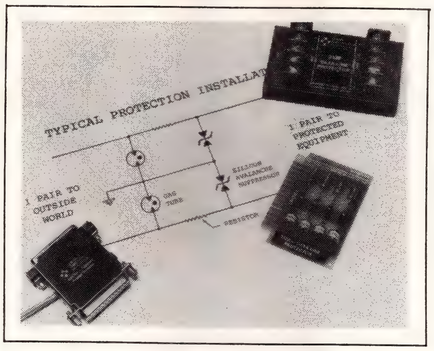
MH&W INTERNATIONAL CORP. 14 Leighton Place, Mahwah, New Jersey 07430 U.S.A. Phone: (201) 891-8800
MH&W INTERNATIONAL (CANADA) LTD. Phone: (416) 676-9401

CIRCLE NO 134

The error rate is less than one per billion bits of data transmitted or received. The modem has its own power supply, which plugs into standard ac sources. $1010.

Honeywell Inc, Honeywell Plaza, Minneapolis, MN 55408. Phone (800) 367-6786; in MN, (214) 234-4271.

Circle No 372


TYPICAL PROTECTION INSTALLATION
1 PAIR TO OUTSIDE WORLD
GAS TUBE
SILICON AVALANCHE SUPPRESSOR
1 PAIR TO PROTECTED EQUIPMENT
RESISTOR

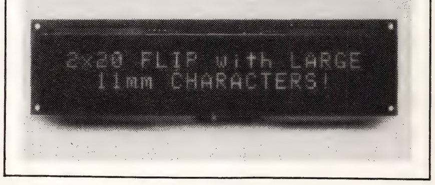
SUPPRESSOR

- *Provides secondary lightning protection*
- *Maximum clamp level is 40V at 75A*

The Model CPP 52 is designed to provide secondary lightning protection for EIA STD RS-232C I/O ports. Intended for indoor use, it incorporates a male and a female 25-pin RS-232C connector. In its standard configuration, it will protect pins 2, 3, 7, and 20; other pin configurations are available. Maximum clamping level is 40V at 75A. Operating and storage range is 0 to 85°C. Two suppressors, one at the CPU and one at the peripherals, protect the system against electrostatic discharge and those switching transients that can be induced or coupled into the data line. You can also use the unit with primary-level protectors located at the service entry when the cable running between the primary protector and equipment is over 10m long. In this arrangement, the primary protector guards against exterior lightning effects while the secondary suppressor protects against indoor transients. $49 (100).

General Semiconductor Industries Inc, Box 3078, Tempe, AZ 85281. Phone (602) 968-3101. TWX 910-950-1942.

Circle No 373



VF DISPLAY

- *Features 2-line×20-character display*
- *Onboard μP*

The Model 3601-40-040 is a 2-line×20-character display that measures 10.8×2.75×1.3 in. The

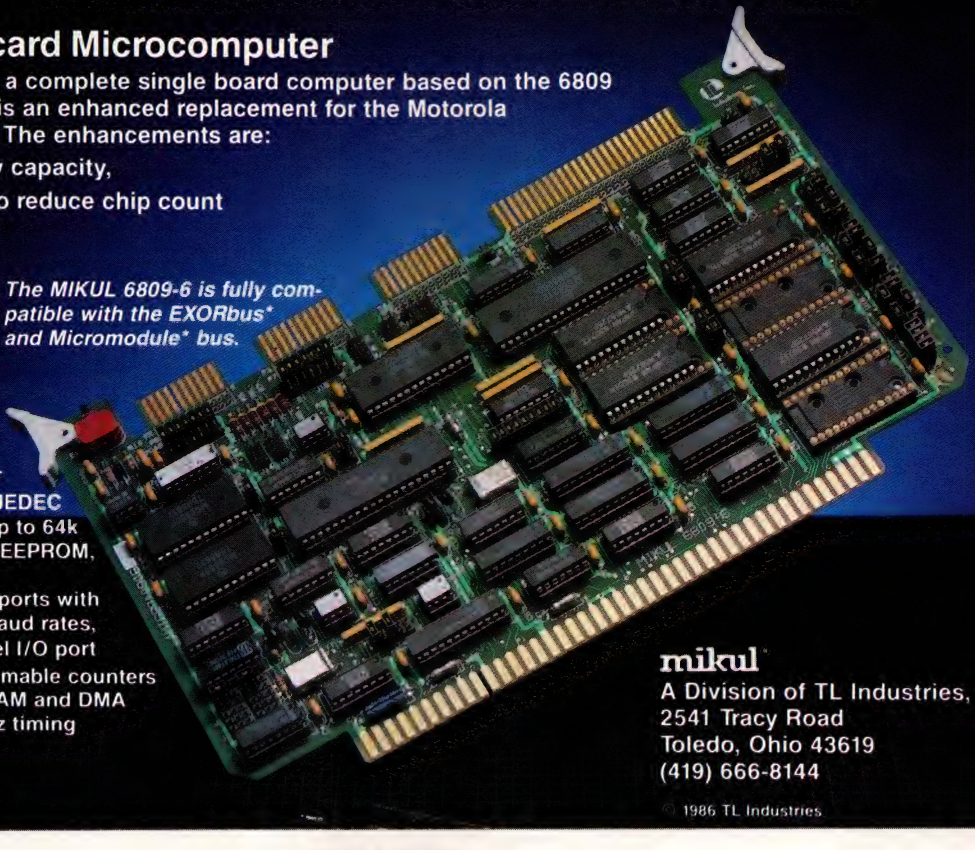
mikul —The Source
for Enhanced Motorola® Micromodule Replacement

6809-6 Monocard Microcomputer

The MIKUL 6809-6 is a complete single board computer based on the 6809 microprocessor and is an enhanced replacement for the Motorola Micromodule* MM17. The enhancements are:

- expanded memory capacity,
- the use of a PAL to reduce chip count

The MIKUL 6809-6 is fully compatible with the EXORbus and Micromodule* bus.*



Features

- 6809 microprocessor
- Six 28-pin standard JEDEC sockets to support up to 64k bytewide static RAM, EEPROM, and ROM devices
- Two RS-232-C serial ports with user selection of 9 baud rates,
- Fully buffered parallel I/O port
- Three 16-bit programmable counters
- Supports dynamic RAM and DMA
- Optional 1.5 or 2 MHz timing
- Power-on reset

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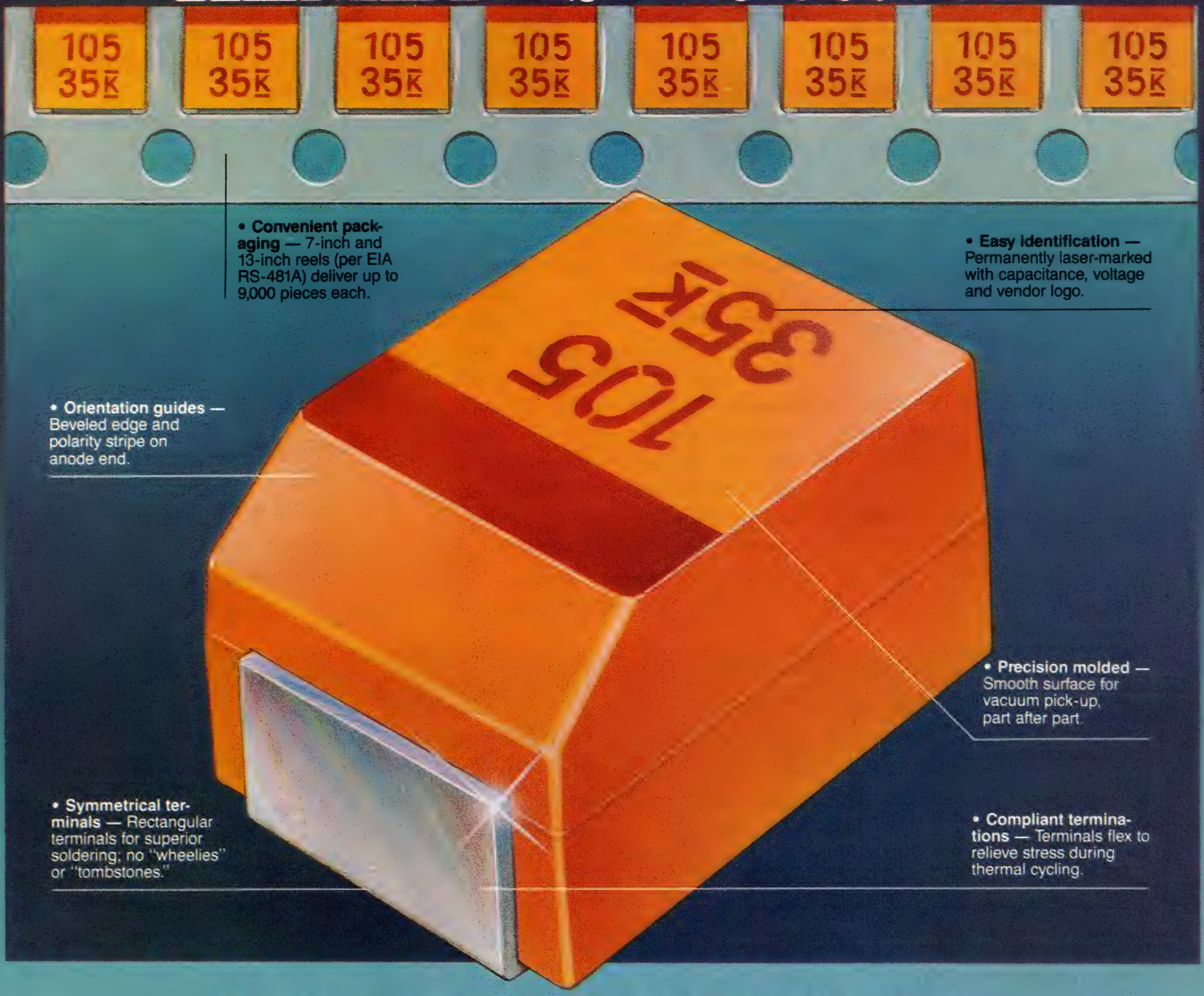
CIRCLE NO 29

TANTALUM CHIPS: KEMET® Is The Source.



- **Convenient packaging** — 7-inch and 13-inch reels (per EIA RS-481A) deliver up to 9,000 pieces each.
- **Easy identification** — Permanently laser-marked with capacitance, voltage and vendor logo.
- **Orientation guides** — Beveled edge and polarity stripe on anode end.
- **Precision molded** — Smooth surface for vacuum pick-up, part after part.
- **Symmetrical terminals** — Rectangular terminals for superior soldering; no "wheelies" or "tombstones."
- **Compliant terminations** — Terminals flex to relieve stress during thermal cycling.

New, High-Production T491 Molded Chip Design: Positive Placement. Simpler Soldering.

Take a close look at the unique, production-boosting features of the new T491 Series surface mount capacitor from KEMET. It's an excitingly different molded tantalum chip design that can increase your production efficiency as it boosts your product reliability:

- **Greater yield** — Designed for high-speed, automatic placement and high-integrity connections.
- **Compatible with all solder reflow methods** — Withstands 260°C for 20 seconds.
- **Meets EIA standards** — Meets or exceeds all IECQ specifications, including QC 300801/US0001.
- **Wide selection** — Capacitances from 0.1 μF to 68.0 μF, and working voltages from 6 to 50 VDC; in case sizes A through D.

They're built to KEMET's unexcelled quality standards with delivery to meet your needs.

For ordering assistance, ask your local KEMET sales office for a T491 Molded Tantalum Chip specification sheet. You'll find it's easy to do business with KEMET!

Sales Offices and Distributors Worldwide
In U.S.A: (803) 963-6348; Telex 57-0496.
In Europe: 41-22-396512; Telex 845-911302.
In Asia: 852-372-31211; Telex 780-45162.

Order KEMET

UNION CARBIDE
ELECTRONICS DIVISION
COMPONENTS DEPARTMENT

CIRCLE NO 172

0.44-in. characters are formed from a 5×7-dot matrix. You can read them easily from a distance of 10 ft. The display requires one 5V dc power supply for operation. An on-board μP controls all of the display functions and interfaces to an 8-bit parallel TTL data bus. A 1200-baud serial interface is also standard for this unit, with jumper selection of either TTL or RS-232C input levels. The module displays the full 96-character ASCII font, as well as additional European characters and scientific symbols. Display characters are blue-green; a spectrum of color filters is available. $210 (100). Delivery, four to six weeks ARO.

IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91405. Phone (818) 787-0311. TWX 910-495-1707.

Circle No 374

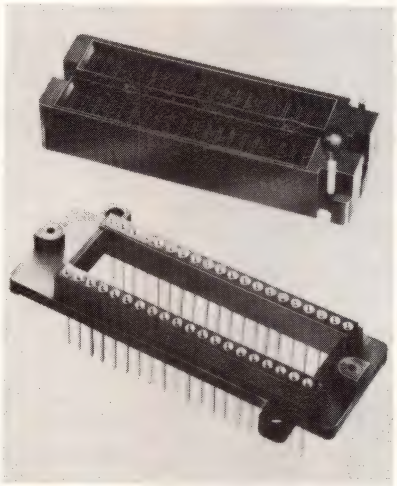
DIGITAL PANEL METERS

- *Display 3½ digits*
- *Input-voltage ranges of ±200 mV, +2V, or ±20V dc*

The DP-900 Series is a family of 3½-digit LCD digital panel meters. Features include low-noise differential inputs, automatic zeroing, 0.1% basic accuracy, and automatic polarity indicator. Models are available with input voltage ranges of ±200 mV, +2V, or ±20V dc. Input impedance is 1000 MΩ, input bias current is typically 1 pA, and common-mode rejection is 86 dB. A hold input allows you to freeze the display reading at any time via a TTL-compatible signal. You can opt for three different positions for the decimal point. Because of extensive use of surface-mount technology, the MTBF, per MIL-HDBK-217, is greater than 500,000 hours. The meters come in 2.3×1.1×0.4-in. bezel-mount cases. Each requires 5V dc at 15 mW. Operation spans 0 to 50°C. $59.

Acculex, One Exeter Plaza, Boston, MA 02116. Phone (617) 267-0800. TLX 240713.

Circle No 375



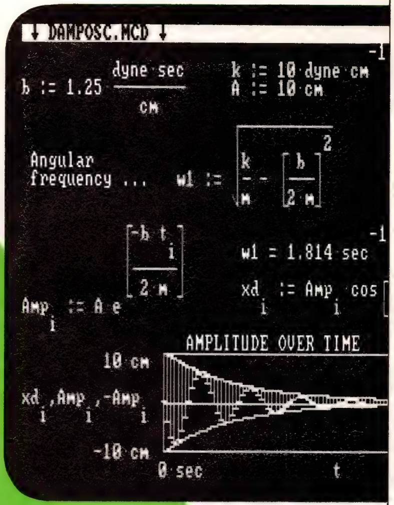
TEST SOCKETS

- *Available in 24-, 28-, 40-, and 48-pin sizes*
- *Feature normally closed design*

The contact area in the Aries line of universal test sockets allows devices on 0.300-, 0.400-, and 0.600-in. centers to be tested. The sockets are available in 24-, 28-, 40-, and 48-pin sizes. The normally closed contact design provides consistent normal force and prevents contact deformation from oversized leads. Contacts are gold- or tin-plated beryllium copper. Other platings and base metals are available for burn-in applications above 150°C. The contacts can accept leads from 0.015 through 0.045 in. wide. Also available is a receptacle with collet contacts, which firmly mounts to the pc board to hold the test socket. Bolts are furnished with the receptacle to connect the socket and the receptacle firmly together. Test socket, 24-pin tin-plated, $3.87; receptacle,

Do math on your PC as easily as writing it down

NEW!



$189

- Enter and display formulas the way you're used to writing them
- Calculate results instantly as numbers or plots
- Change anything—results are automatically recalculated
- Real and complex numbers, unit conversions, dimensional analysis
- Add text anywhere to document your work
- Print out everything just as you see it

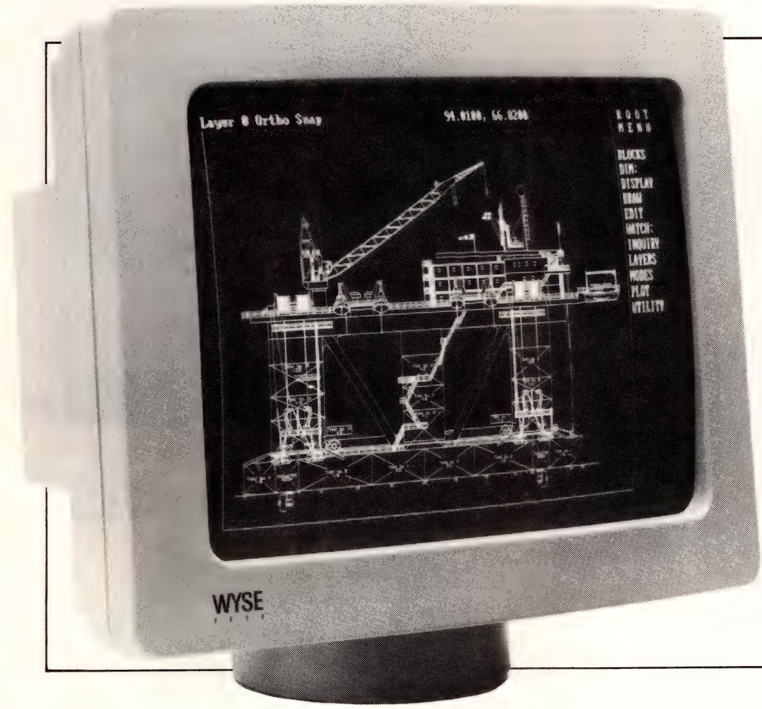
MathCAD

The Engineer's Scratchpad

MathSoft Inc.
One Kendall Square
Cambridge, Massachusetts 02139

1 800 MathCAD or 617 577-1017

Wyse takes the high cost out of high resolution.



At $999, the WY-700 Graphics Subsystem is easily affordable. And its 1280 x 800 resolution makes the best of software packages like these:

DESKTOP PUBLISHING
Ventura Publisher
PageMaker/PC
Frontpage
DeskSet
Pagemaster
Rim System
Compound Document Processor
Display Ad Make-up System
AdvanTex

GENERAL PC SOFTWARE
Lotus 1-2-3
Symphony
PC-Paintbrush

COMPUTER-AIDED DESIGN
AutoCAD
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WYSE

YOU NEVER REGRET A WYSE DECISION.

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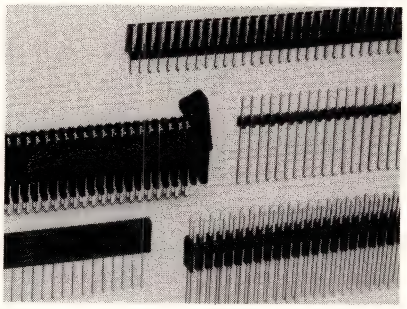
24-pin gold collet, tin shell, $3.62 (100).

Aries Electronics Inc, Box 130 Frenchtown, NJ 08825. Phone (201) 996-6841.

Circle No 376



HEADER/SOCKETS

- *Standard sizes of 36/72 pins with single/double row*
- *Strips snap to smaller lengths*

These 0.025-in.-square post headers and sockets are available in a variety of body styles. You can order the strips in standard sizes of 36 pins for a single row and 72 pins for a double row. For shorter lengths, you can use the break-away feature to snap strips to desired length down to even one or two positions. Strips are available shrouded or unshrouded, straight or right angled, and in a 1- or 2-row design. Plating is gold, tin, or selective gold/tin. Body material is Dupont Rynite PET polyester suitable for high-temperature soldering applications. From $0.03 (1000).

Samtec Inc, Box 1147, New Albany, IN 47150. Phone (812) 944-6733. TLX 333918.

Circle No 377

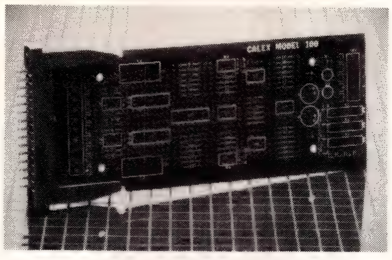
PROTOTYPE CARD

- *Features a variety of hole patterns*
- *Includes a 15-pin edge connector*

The Model 100 Protocard has hole patterns for 16- and 8-pin DIPs, potentiometers, resistors, capacitors, diodes, and transistors. It also has hole patterns for wire-wrapped pins for point-to-point wiring of prototypes. A silk-screened guide on the surface identifies the location of 70 different components. The device comes with a 15-pin edge connector that has built-in card guides. The card is also available with barrier-strip style termination. $29.50.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911. TLX 338506.

Circle No 378



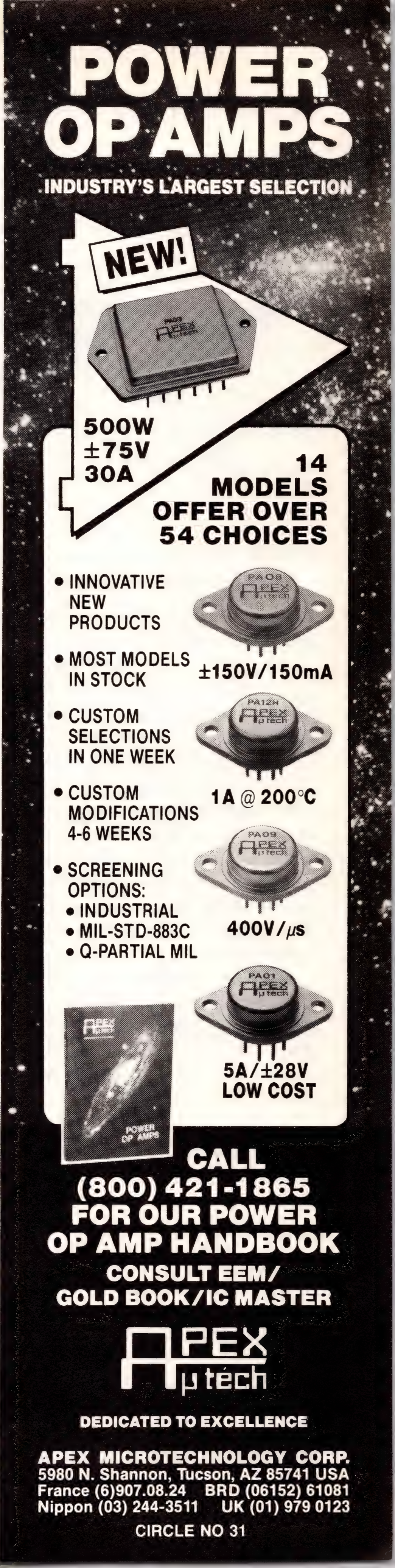
PANEL METER

- *Takes up <4 in² of board space*
- *Five pin-selectable ranges*

The Series G920 Mini Versameter requires less than 4 in² of panel space. This 3½-digit unit has a 0.5-in. LED display. The panel meter features five built-in, pin-selectable dc-voltage or -current ranges from 200 mV to 1000V or 200 μA to 2A full scale. It requires 5V dc at 150 mA. A 4- to 20-mA model is also available that you can scale into specific engineering units using offset and span adjustments accessible through the rear of the case. The meter comes with card edge connector. $69; 4- to 20-mA model (G922), $79.

Extech Instruments Corp, 150 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. TLX 940913.

Circle No 379



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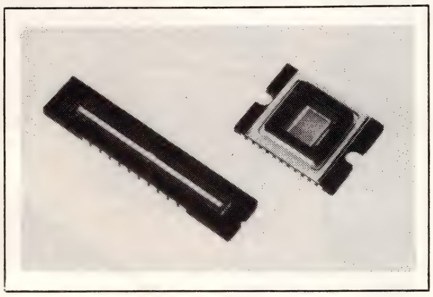
CIRCLE NO 31

NEW PRODUCTS

ICs & SEMICONDUCTORS



CCD SENSORS

- *Linear sensors have 128 to 5000 elements*
- *Area sensors have 40×14-, 488×376-element arrays*

The manufacturer's linear CCD sensor line consists of seven devices having 128 to 5000 elements. Each sensor operates from a 12V supply. Two area CCD sensors have 40×14- and 488×376-element arrays. They operate from single 8 and 15V supplies, respectively. The sensors offer high resolution, and elements measure as little as 7 µm per side. They accommodate operating frequencies as high as 10 MHz. In hermetically sealed packages, from $25 to $285 (100). Delivery, 10 to 12 weeks ARO.

Toshiba America Inc, Semiconductor Products Div, 2692 Dow Ave, Tustin, CA 92680. Phone local office.

Circle No 380

FILTER ICs

- *Seventh-order elliptic filters*
- *Provide 70-dB min stopband rejection*

Models XR-1015 and XR-1016 filter ICs are seventh-order elliptic lowpass filters. They provide stopband rejection of greater than 70 dB; consequently, they minimize out-of-band noise. The devices operate from single 5V supplies. You can use them with an A/D converter or with a digital circuit for the generation of a sine wave from a 25-kHz max square wave. The XR-1016, unlike the XR-1015, has two operational amplifiers you can use as anti-aliasing filters, as allpass filters, or for gain adjustment. Both devices operate over 0 to 70°C. The XR-1015, in a plastic or ceramic 8-pin DIP, $4.95; the XR-1016, in a plastic or ceramic 14-pin DIP, $5.69 (1000).

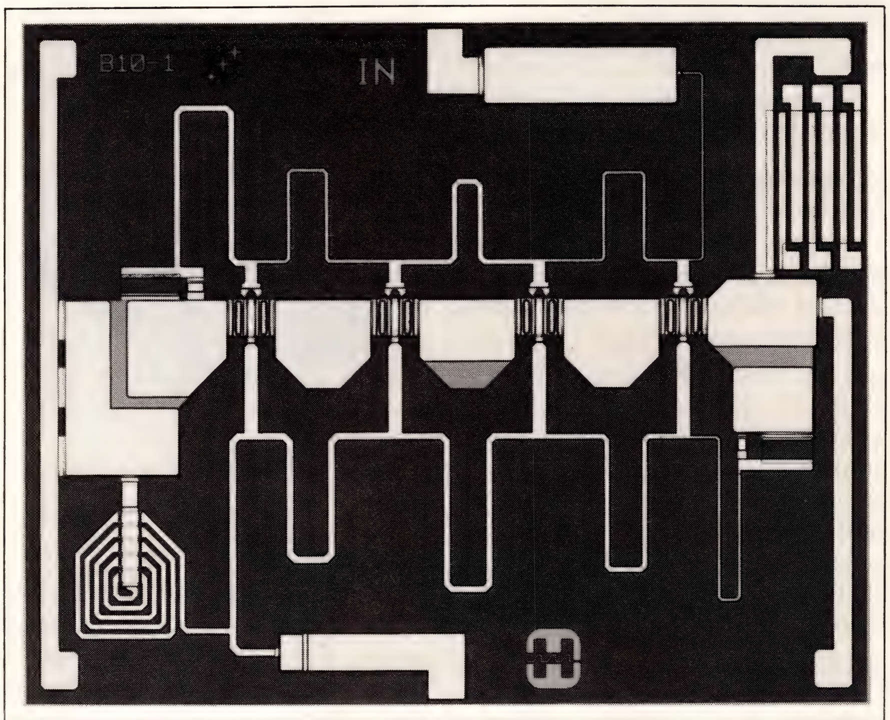
Exar Corp, Box 3575, Sunnyvale, CA 94088. Phone (408) 732-7970. TWX 910-339-9233.

Circle No 381

ANALOG PROCESSOR

- *Has on-chip transmit modulation*
- *Provides programmable transmit-level control*

The SSI 214 IC is the first IC provided as a direct interface to a standard DSP, according to the manufacturer. The device features on-chip transmit modulation, DTMF generation, call-progress detection, answer tone, and carrier detection. It also accommodates



GaAs MMIC

- *Operates over 6 to 18 GHz*
- *Available in die form*

The HMM-11810-0 0.5-µm GaAs monolithic microwave IC (MMIC) amplifer operates over a 6- to 18-GHz frequency band. According to the manufacturer, the device is the first fully cascadable amplifier available in die form. It includes on-chip dc-blocking and bypass functions, which make it directly cascadable. The amplifier features a signal gain of 5 dB and gain flatness of 0.75 dB across its frequency range. The I/O VSWR is 2:1 max. Its typical noise figure at 50 mA and 18 GHz is 6 dB. The device has short-circuit protection, large gold bonding pads, and a Ti/Pt/Au metallization system. The amplifier's variable bias capability allows gain-, power-, and noise-optimized operation. $200 (100). Delivery, six weeks ARO.

Harris Microwave Semiconductor, 1530 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 262-2222.

Circle No 382

Hyspeed from Hybrid

Hybrid Systems' new CMOS Flash Converters and High Speed Hybrids provide an unbeatable combination of speed and uncompromising quality.

Now, Hybrid Systems brings its 20-year reputation for high quality, high reliability, and high performance to a new line of high speed products. Our monolithic flash converters and high speed hybrids are designed to meet the needs for fast digitizing and low power consumption in the most demanding real time data acquisition and analysis applications.

ANALOG TO DIGITAL

	RESOLUTION	CONVERSION TIME	POWER
HS9582*	6-bits	40 nsec	150mW
HS9583*	8-bits	200 nsec	75mW
HS9584*	8-bits	50 nsec	300mW
HS9520	12-bits	2.0 μsec	1.2W

DIGITAL TO ANALOG

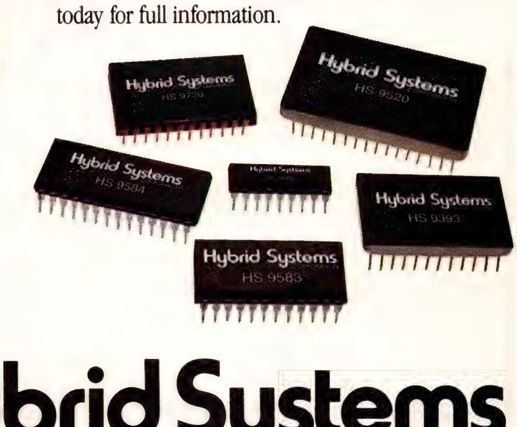
	RESOLUTION	SETTLING TIME	POWER
HS9393	12-bits	50 nsec	495mW

SAMPLE AND HOLD

	RESOLUTION	ACQUISITION TIME	POWER
HS9720	12-bits	200 nsec	765mW

*Flash Converters

All high speed components meet commercial and military temperature ranges. All products for military applications are processed to MIL-STD-883. Better still, all carry a name that is synonymous with expertise, reliability, and unsurpassed customer service: Hybrid Systems Corporation. Contact us today for full information.

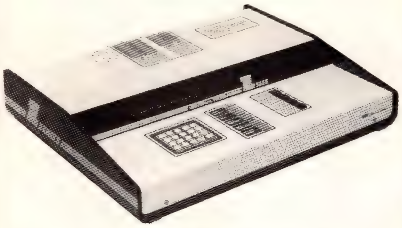


Hybrid Systems
CORPORATION

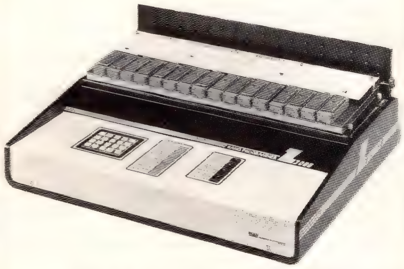
22 Linnell Circle, Billerica, MA 01821 617-667-8700

CIRCLE NO 154

AMERICA'S BEST PROGRAMMERS



Z-1000B UNIVERSAL PROGRAMMER
- Over 600 PLDs, EPROMs, EEPROMs, Bipolar PROMs and INTEL MCUs.
- Separate D/A channels for each pin.
- Upgradeable PROM based software.
- Stand alone or PC/XT/AT operation.
- Two independent RS-232 ports.
- 64K or 256K bytes of DATA RAM.
- EXATRON handler interface is standard.



Z-3000 HIGH VOLUME GANG/SET PROGRAMMER
- 14,000 27256s programmed per day.
- 32 EPROMs simultaneously with 1 to 8 DATA BLOCKS.
- 16 Intel or Motorola MCUs at a time.
- 64K to 256K bytes of DATA RAM.

Z-1200B TWELVE SOCKET GANG/SET PROGRAMMER
- 2716 – 27512, 1 to 4 DATA BLOCKS.
- 64K to 256K bytes of DATA RAM.
- Software personality. No plug-ins.

Z-2500B IN-CIRCUIT MEMORY CARD PROGRAMMER
- Programs up to 32 memory cards with EPROMs or microcomputers at a time.
- Two 1.2 Mbyte DSDD floppy disk drives. Optional 20 Mbyte hard disk.
- Turnkey systems include programmer, terminal, custom interface hardware and software.
- Simple menu driven operation.

ZAP SERIES engineering and field service programmers for EPROMs to 27C1024, Intel and Motorola microcomputers.

Z-400 economical bipolar PROM and EPROM programmer.

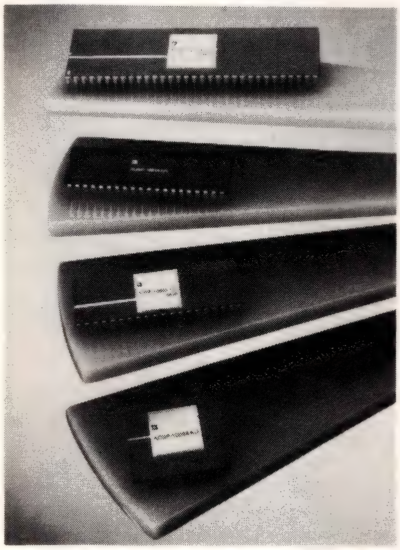
SUNRISE ELECTRONICS, INC.
524 South Vermont Avenue
Glendora, California 91740
(818) 914-1926

CIRCLE NO 36

2400-, 1200-, 600-, and 300-bps operating modes, programmable transmit-level control, an on-chip timer, and a speaker-monitor output. You can encode your own DSP to use with the SSI 214, or you can purchase a complete chip set from the manufacturer consisting of an SSI 214, a precoded 77C20 DSP, and Hayes-compatible firmware source code for an 8051/8031. It's available in a 28-pin DIP or a PLCC surface-mount package. SSI 214 DIP, \$19.95; 2-chip set (SSI 214, 77C20) and 8051 firmware source code, \$34.95 (OEM qty).

Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110.

Circle No 383



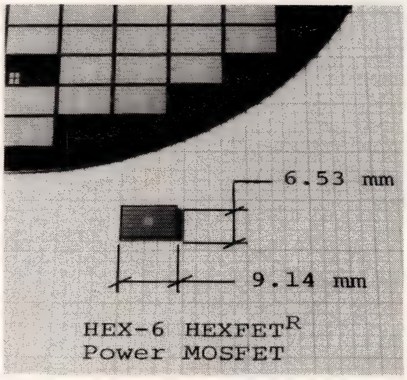
MULTIPLIERS

- *Multiplication rates of 30 and 20 MHz*
- *Consumes <1⁄10 the power of compatible ICs*

Four 1.5-μm upgrades of the company's earlier line of 5-μm CMOS multipliers and multiplier/accumulators include the ADSP-1080A, ADSP-1081A, ADSP-1012A, and the ADSP-1009A. According to the company, they're faster than the parts they replace yet they consume less than 10% of the power. The ADSP-1080A and -1081A 8×8-bit multipliers feature multiplication rates of 30 MHz. Power dissipation for both devices is 275 mW max. Both are available in 40-pin ceramic and plastic DIPs. The ADSP-1012A and ADSP-1009A address requirements for 12-bit computation. The ADSP-1012A 12×12-bit multiplier operates at a 20-MHz rate and consumes 300 mW max. The -1009A multiplies and accumulates a product at a 70-nsec rate and consumes 350 mW max. Both are available in 68-lead pin-grid arrays and 64-pin ceramic or plastic DIPs. In plastic DIPs, from \$27 to \$53.30 (100). Delivery, four weeks ARO.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 461-3881.

Circle No 384



POWER MOSFET

- *Switches 18 kW of power*
- *Dissipates 350W at T_C=25°C*

The IRF460 HEX-6 500V power-MOSFET die specs a 0.225Ω $R_{DS(ON)}$. It can shut off 18 kW of power within 10 nsec. The device has a rated V_{DS} of 500V, conducts 24A drain current, and can dissipate 350W at a 25°C case temperature. In an all-copper military TO-3 package, \$69.45. In the fourth quarter of 1986, the device will be available in a TO-247AB plastic commercial package.

International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8814.

Circle No 385

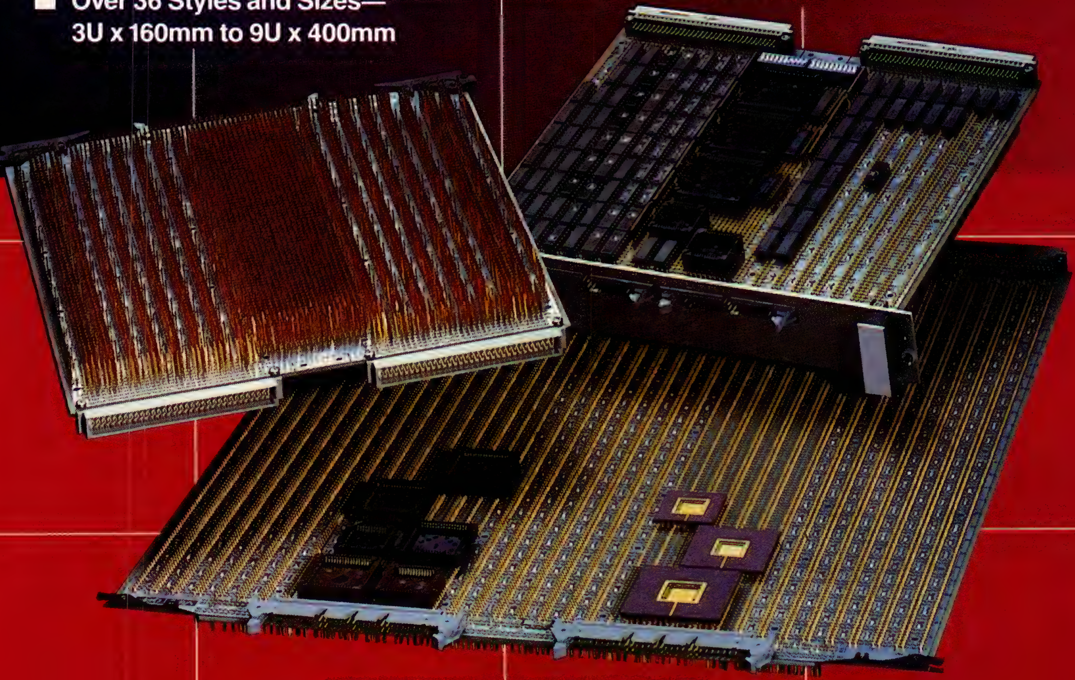
VECTOR LOGICpak *plus*

THE BEST
High Speed, DIN Based Logic Boards

Advanced Features:

- Usable to 250 MHz
- High Density—More ICs per Board
- Optimized Distributed Capacitance
- Wire Wrap and Low Profile Stitch Wire
- DIN/Eurocard, VMEbus, Multibus® II Formats
- Over 36 Styles and Sizes—
  3U x 160mm to 9U x 400mm

Schottky Boards
Four-layer boards enhance high speed performance and decrease power plane impedance.



SMD Decoupling Capacitors
Reduce inductance due to leaded parts and eliminate wiring tool interference.

High Speed Universal Boards
Versatile boards for mixing TTL, CMOS, analog and even ECL on the same board.

Vector Electronic Company introduces *LOGICpak Plus™* —a new line of advanced, high speed, high density logic boards.

HIGH SPEED performance is achieved through the use of SMD capacitors and four-layer construction with inter-pin planes and inter-layer connections.

HIGH DENSITY packaging results from an efficient socket pin pattern that allows more ICs to be mounted per board and patterns that accommodate PGA and LCC devices.

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VECTOR
ELECTRONIC COMPANY

CIRCLE NO 204

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- **WITH UP TO 95% EFFICIENCY**

Melcher switching power supplies are ideal for control systems, telecommunications and military applications and are available in PCB module, chassis mount, 19" rack, and Eurocard configurations.

Reduce the overall cost of ownership for your power supply with the quality and reliability built into every Melcher product.

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CIRCLE NO 37

Technacell™

SEALED LEAD ACID

Elpower's line of Technacell maintenance-free sealed lead acid batteries offer high performance in all cyclic and stand-by applications. Fully rechargeable, these batteries are available in a range of 2 volts through 12 volts and are capable of having up to 1000 cycles!

But Elpower offers you much more than just quality sealed lead acid batteries — they also happen to be experts in the areas of on time delivery, quality assurance, and competitive pricing! So when reliability counts most, count on Elpower, the battery experts!

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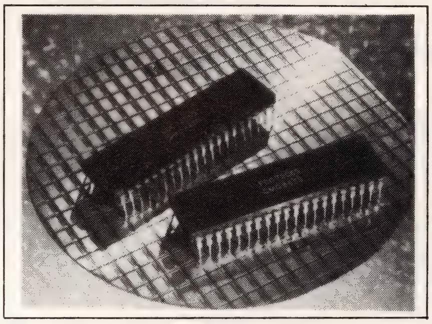
CIRCLE NO 38



DISK CONTROLLER

- *Increased recalibration step limit from 77 to 255*
- *Controls as many as four drives*

The FDC72C65 disk controller is an enhanced, pin-compatible version of the industry-standard FDC765A. The device can provide an interface for a processor and four floppy-disk drives in single or double density. It accommodates the IBM 3740 single-density format or IBM System 34 double-density format. You can program the device for low-power operation when the disk drive is not in use. Combined with the FDC92C39 data separator, the subsystem draws only 30 mA. It features an increased (from 77 to 255) recalibration step limit and enhanced DMA timing. The device requires a single 5V power source. In a 40-pin plastic DIP, $15 (1000). Delivery, four to six weeks ARO.

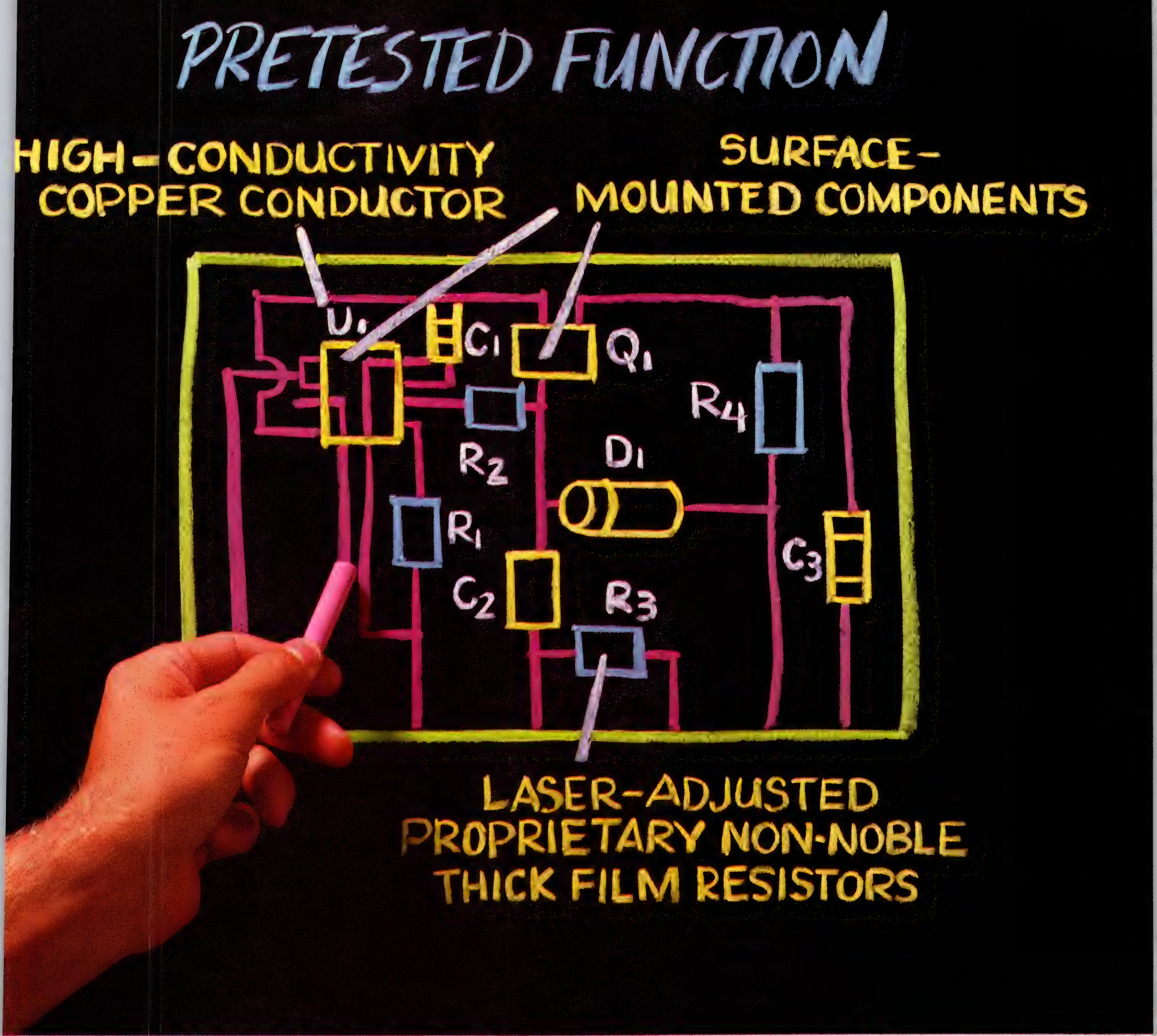
Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 273-3100.

Circle No 386

BUFFER IC

- *Supplies current drive at 300 MHz*
- *Pin compatible with Harris's HA5033*

The VA033 unity-gain video buffer amplifier features a slew rate of 2000V/μsec. It has an operating voltage of ±5V and can supply current drive at frequencies exceeding 300 MHz. The device can be used as an op-amp isolation buffer for driving reactive loads or as a high-im-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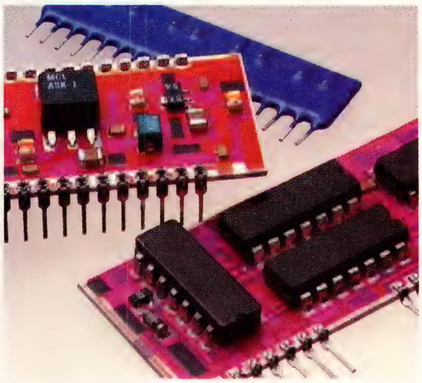

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CIRCLE NO 174

pedance input buffer for use with high-speed A/D converters and comparators. It has an output drive of ±100 mA and can drive 25Ω loads and 50Ω terminated transmission lines. The device is pin compatible with Harris's (Melbourne, FL) HA5033 and National's (Santa Clara, CA) LH0033. $8.90 to $14.90, depending on package type. (100).

VTC Inc, 2401 E 86th St, Bloomington, MN 55420. Phone (612) 851-5000.

Circle No 387

EPROM

- *Supported by Intelligent Programming algorithm*
- *Provides an interface without wait states*

The JD27256 EPROM provides an interface without wait states to high-performance μPs such as Intel's M80186. The device is supported by the Intelligent Programming algorithm. Using this algorithm, you can program the IC in six minutes. The IC ensures the program's reliability by performing a checking sequence on each bit. In a 28-pin JEDEC-approved package, $72 (10,000).

Intel Corp, Box 59065, Santa Clara, CA 95052. Phone (602) 961-8375.

Circle No 388

STATIC RAMs

- *Operate from single 5V supply*
- *Operate to LV-TTL JEDEC Standard 3.3V*

The MK41H68, MK41H69, and MK41H78 comprise a family of CMOS static RAMs. The -41H68 4k×4-bit memory has a 20-pin pinout and 20-nsec address time. It includes a chip-enable power-down feature that reduces power to less than 50 μA in standby. The -41H69 features a chip-select access time of 10 nsec. The -41H78 features maximum output-enable access times as fast as 10 nsec. All the devices operate from a 5V supply. They are available in low-voltage versions that operate from the LV-TTL JEDEC standard 3.3V supply, and are the first LSI LV-TTL memories to be introduced to the market, according to the manufacturer. Full static operation requires no external clock or refresh and ensures low operating and standby power dissipation. MK41H68, in a ceramic package, $34.30 (100).

Thomson Components-Mostek Corp, 1310 Electronics Dr, Carrollton, TX 75006. Phone (214) 466-6000.

Circle No 389

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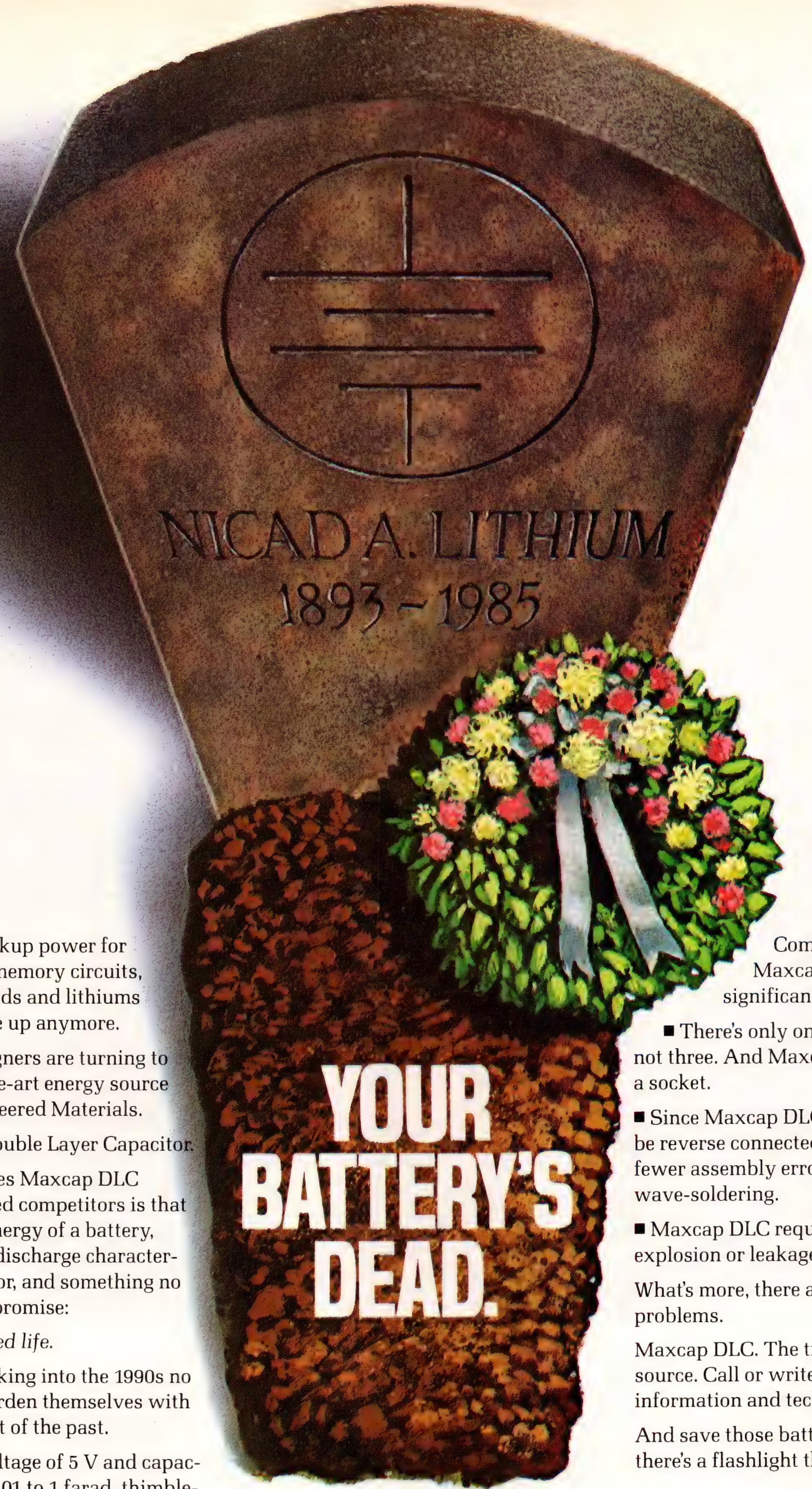
CIRCLE NO 39



As backup power for CMOS memory circuits, the ni-cads and lithiums just don't measure up anymore.

Now, circuit designers are turning to a new, state-of-the-art energy source from Sohio Engineered Materials.

The Maxcap™ Double Layer Capacitor.

What distinguishes Maxcap DLC from its antiquated competitors is that it gives you the energy of a battery, the rapid charge-discharge characteristics of a capacitor, and something no battery can ever promise:

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Compared to batteries, Maxcap DLC delivers these significant cost savings:

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- Maxcap DLC requires no toxicity, explosion or leakage safeguards.

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Sohio Engineered Materials Company
Semiconductor Products Division
P.O. Box 664
Niagara Falls, NY 14302
716/278-3954

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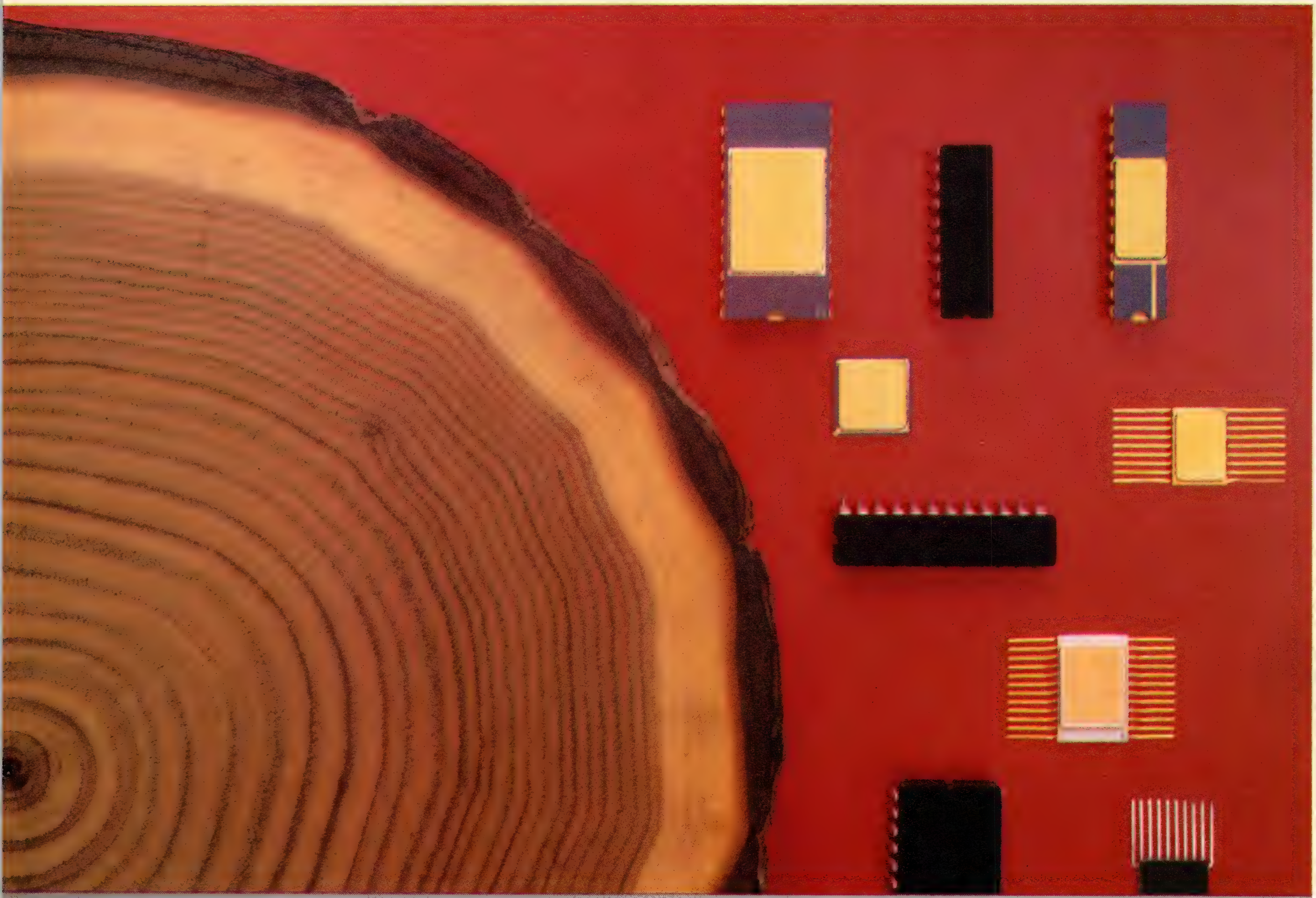
Maxcap DLC shown actual size above.

CIRCLE NO 184

Bipolar PROMs Through Thick & Thin.



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CIRCLE NO 205

NEW PRODUCTS

COMPUTER-SYSTEM SUBASSEMBLIES

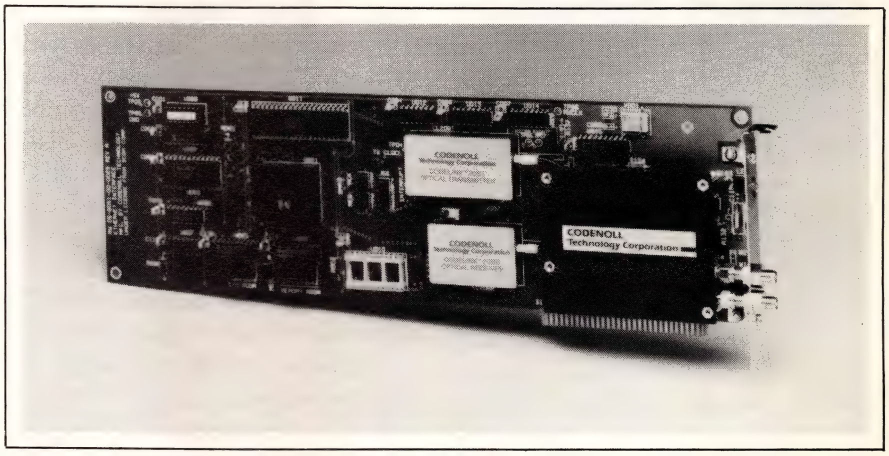
FIBER-OPTIC ADAPTER

- *Lets PCs drive Ethernet networks*
- *Communicates over a 2000m distance*

The CN-3051 adapter board, operating on a fiber-optic network, allows an IBM PC, PC/XT, PC/AT, or compatible computer to communicate over distances as great as 2000m. The board has a transmitter and a receiver that are compatible with 3Com's (Menlo Park, CA) version of Ethernet. The onboard fiber-optic modules are compatible with IBM's fiber-optic cabling system, AT&T's fiber-optic premise distribution system, and the manufacturer's Focus system. The board operates at data rates as high as 10M bps. The board's digital and PC Bus sections support 3Com's 3Plus and EtherSeries software and Novell's (Orem, UT) Netware software. $995.

Codenoll Technology Corp, 1086 N Broadway, Yonkers, NY 10701. Phone (914) 965-6300. TLX 646159.

Circle No 390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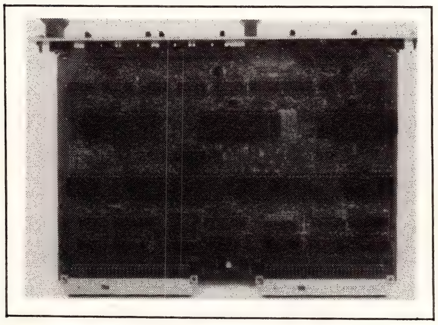


MOTOR CONTROLLER

- *Operates on the VME Bus*
- *Drives as many as three motors*

The DMC-300 Series programmable motion controller lets you control as many as three dc or brushless dc motors simultaneously. The VME Bus-compatible card governs point-to-point positioning, error handling, and status reporting for the motors it controls. An onboard µP executes a control algorithm every 0.5 msec. The controller accepts feedback information from rotary or linear-incremental encoders; it provides stable control with or without a tachometer feedback loop. When operating without tachometer feedback, a digital filter lets you adjust its coefficients for optimum motor performance. High-level commands specify position, speed, acceleration rate, and compensation for each motor. DMC-300 (one axis), $645; DMC-320,(two axes) $1195; DMC-330 (three axes), $1695.

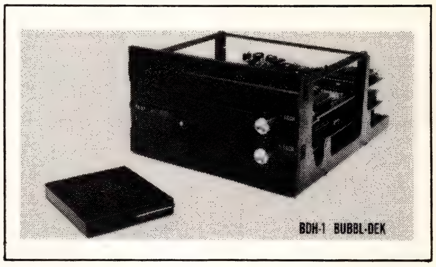
Galil Motion Control Inc, 1928-A Old Middlefield Way, Mountain View, CA 94043. Phone (415) 964-6494.

Circle No 391

BUBBLE MEMORY

- *Replaces floppy-disk drives*
- *Features a redundant bit-encoding technique*

The BDH-1 Bubbl-Dek system fits in the same mounting holes as a standard full-height 5¼-in. floppy-disk drive. The unit has either one or two slots for plug-in bubble-memory cartridges, and each cartridge stores 128k bytes of data. A redundant bit-encoding technique lets the controller detect errors. The controller performs retry operations when it detects soft errors. You can choose from controllers for standard computers based on the LSI-11 bus, VME Bus, STD Bus, Multibus, Versabus, and buses for the IBM PC family. An optional interface lets you operate the bubble memory's controller as an RS-232C or RS-422 peripheral at standard data rates as high as 38,400 bps. Memory-access times are as fast as 11.25k bytes/sec. $1324 (10).



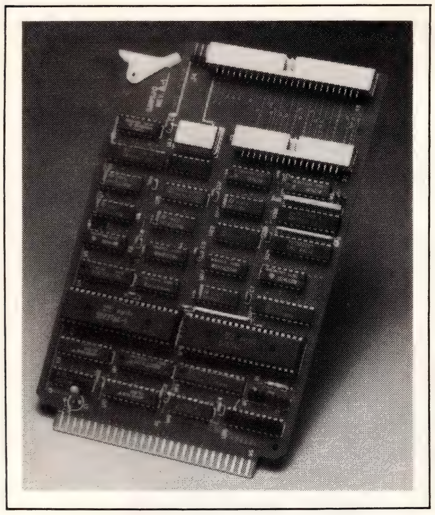
Bubbl-Tec, 6805 Sierra Ct, Dublin, CA 94568. Phone (415) 829-8700. TWX 910-389-6890.

Circle No 392

DISK INTERFACE

- *Supports STD Bus CPUs*
- *Connects as many as four floppy-disk drives to a system*

After adding an SB8520 card to your STD Bus computer system, you'll be able to connect as many as



four 8-, 5¼-, or 3½-in. floppy-disk drives to the system. The card provides a 50-pin connector for 8-in. disk drives and a 34-pin connector for other drives. The control software lets you access each type of drive from your programs without first changing cables or jumpers. The board's DMA controller supports 16-bit addressing for Z80, 8085, 6502, and other 8-bit µPs. You can also select 20-bit addressing for such µPs as the 8088 and 68008. The board is optimized for operation with 8088-based STD Bus computers. $295 (25).

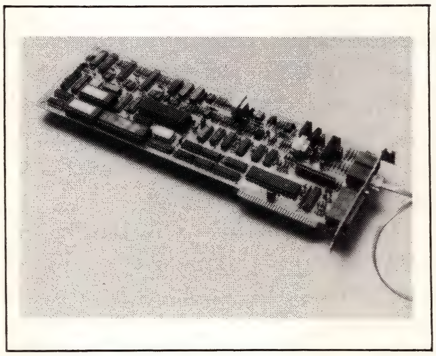
Micro/sys, 1011 Grand Central Ave, Glendale, CA 91201. Phone (818) 244-4600.

Circle No 393

SDLC MODEM

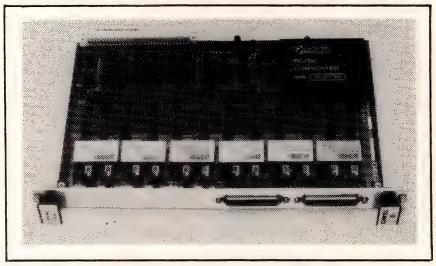
- *Communicates at 4800 bps*
- *Runs on IBM PCs*

The AdaptModem 4800, a combination synchronous modem and synchronous data-link control (SDLC) adapter, runs in the IBM PC, PC/XT, PC/AT, or compatible computers. The plug-in board includes an onboard Bell-208-compatible synchronous modem that operates at 4800 bps. An RJ-11 modular connector lets you make a direct connection to a phone line. The SDLC portion of the board includes all the circuits necessary for interfacing directly to an SDLC line. The modem comes complete with the manufacturer's automatic-call-control (ACC) software, which includes autodial, autoanswer, automatic redial, and modem-test procedures. The software also maintains a 180-phone-number directory for speed dialing or automatic, unattended operation. $1195.



Network Software Associates Inc, 22982 Mill Creek, Laguna Hills, CA 92653. Phone (714) 768-4013.

Circle No 394

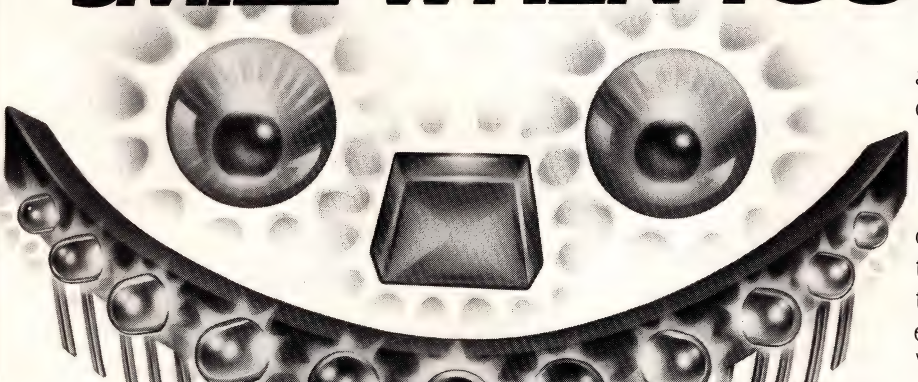


DAC BOARD

- *Furnishes six channels*
- *Supplies 16-bit resolution*

The DVME-626 board guarantees 14-bit monotonicity within a 15-µsec settling time, according to the manufacturer. It provides six DAC output channels. Accuracies for all six outputs are greater than 0.005% of full scale. You can select two versions of the basic board that put out different ranges: The DVME-626V1 has a ±10V range; the DVME-626V2's range is 0 to 10V or ±5V. Both boards accept data in bipolar 2's-complement, bipolar offset-binary, or unipolar straight-binary formats. All DACs are reset to 0.00V

SMILE WHEN YOU SAY IDI



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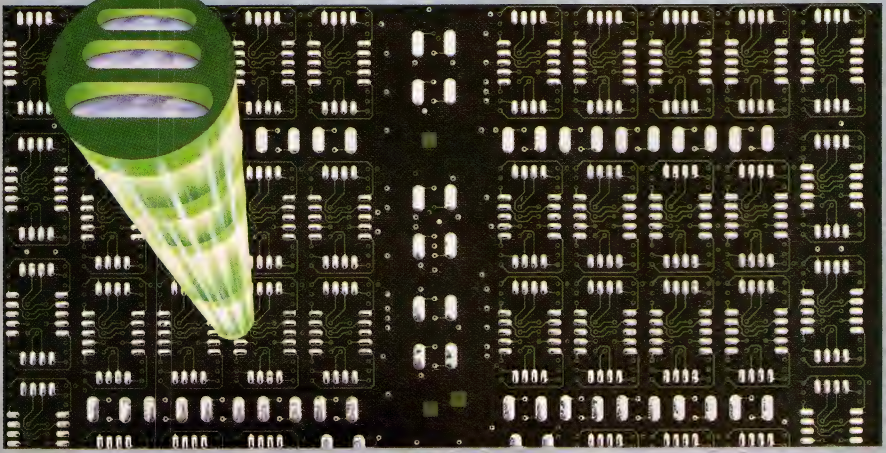

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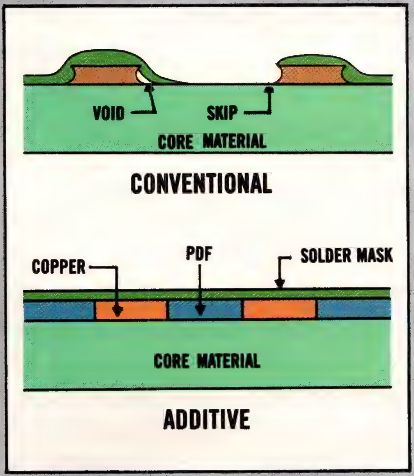

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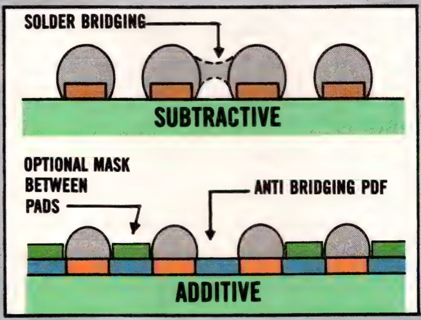

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CIRCLE NO 148

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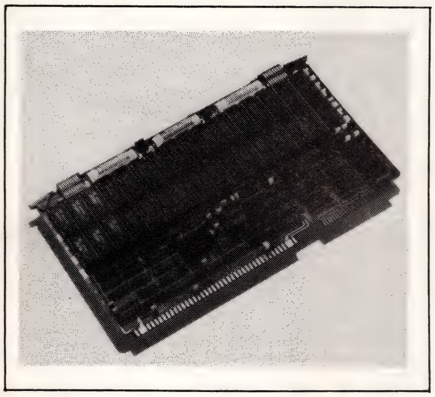
CIRCLE NO 46

output when the computer system is reset, regardless of the data format you select. The boards respond to short I/O addresses, and onboard switches select the base address for each board. The I/O address space maps into 256-address boundaries on the VME Bus's short (64k) I/O space. Both models of the basic board include an onboard dc/dc converter that obtains power from the 5V supply on the VME Bus. $1768.

GE/Datel, 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-9341. TWX 710-346-1953.

Circle No 395



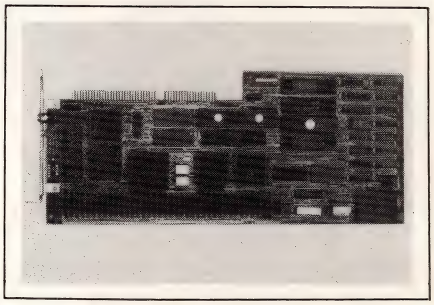
MEMORY BOARD

- *Supplies as much as 1M byte of memory*
- *Supports Multibus*

The MM-7400C memory board, which is compatible with Multibus/iLBX systems, operates with 80286, 80186, or 68000 μPs. You can populate the board with either 8k- or 32k-byte CMOS RAM chips, thus providing memory capacities of 64k to 1M bytes. Two independent memory blocks let you mix RAM and EPROM chips that have the same memory capacity. Three onboard, redundant, fused lithium or NiCd batteries provide nonvolatile operation of the RAMs. A power-fail circuit automatically switches the batteries on when they're needed to power the RAM chips. Lithium batteries allow the memories to retain data for three years; NiCd batteries, for four weeks. From $725.

Micro Memory Inc, 9540 Vassar Ave, Chatsworth, CA 91311. Phone (818) 998-0070.

Circle No 396



CPU BOARD

- *Supplies 1M byte of RAM*
- *Plugs into IBM PC/AT*

The Model B286 CPU card is a single-board industrial computer that plugs into a passive IBM PC/AT mother board or backplane in an IBM PC/AT (or into the equivalent Model 7531 desktop or Model 7532 rack-mount computers). The card provides 1M byte of RAM, and it runs at 6- and 8-MHz or 6- and 10-MHz clock speeds (selectable from an attached keyboard). An onboard battery provides backup for the CMOS RAM and the real-time clock/calendar. The CMOS RAM stores configuration data for the setup program, which is in ROM. The card has keyboard and speaker interfaces, a reset switch, an external speaker jack, and a socket for an 80287 math processor. Less than $1000 (100).

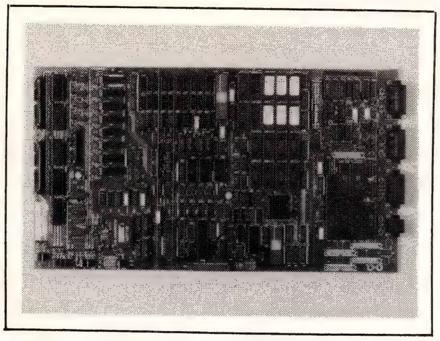
Texas Microsystems Inc, 10618 Rockley Rd, Houston, TX 77099. Phone (713) 933-8050.

Circle No 397

CONTROLLER BOARD

- *Contains onboard software*
- *Controls and monitors analog and digital devices*

The 16-bit single-board Sentinel computer controls analog and digital devices and monitors analog and digital inputs. The analog section multiplexes 30 true-differential analog inputs to a 16-bit successive-



approximation ADC. An 8-channel DAC provides 12-bit resolution. The board also provides as many as 80 TTL-compatible I/O lines. The board accepts programming in the manufacturer's Dabil language, which is similar to Basic. The computer controls an external RS-232C-compatible terminal, which you use for programming. The board's 512k bytes of RAM store data and program steps. For the prevention of program and data loss during power failure, 256k bytes of RAM are battery backed. $4500.

CompuDas Corp, Box 4688, Ithaca, NY 14852. Phone (607) 257-3003. TLX 650-249-8942.

Circle No 398

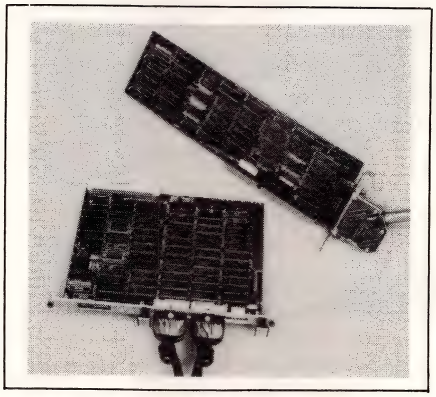
BUBBLE CARD

- *Requires one PC expansion slot*
- *Emulates a hard disk*

Fitting into a single expansion slot in an IBM PC, PC/XT, PC/AT or compatible computer, the iPCB-76 PC-Bubble card emulates a hard disk. The card operates with one or two of the manufacturer's 4M-bit bubble-memory devices and stores as much as 1M byte of information. The card contains the bubble-memory controller, a bus interface, I/O interface logic, and an EPROM-based I/O driver. The EPROM's BIOS (basic I/O system) software lets the memory emulate a hard disk. Specialized software also makes the memory compatible with all versions of MS-DOS and PC-DOS. When transferring data, the card draws 2.6A; in its standby mode, it draws 0.8A. The maximum transfer rate is 50k bytes/sec. Because the storage medium is bubble memory, the board can withstand harsh environmental conditions and mechanical shock as high as 5g while operating. 1M-byte version, $1445; 0.5M-byte version, $795 (100).

Intel Corp, Literature Dept #W-316, Box 58065, Santa Clara, CA 95052. Phone (916) 351-2746.

Circle No 402



VME BUS ADAPTER

- *Drives an IBM PC/AT or compatible computer*
- *Acts as a bus master or slave*

The Adaptor is a set of two pc boards that lets you link a VME Bus system to an IBM PC/AT or compatible computer. Cable lengths between the two computer systems can range from 8 to 50 feet. The PC/AT can communicate with the VME Bus computer in three ways: by direct addressing, by page-mode addressing, and by dual-port RAM addressing. The PC/AT operates as a bus master or as one of several masters in a multiprocessing computer system. Address mapping lets the PC/AT address as many as 14M bytes of VME Bus memory as if the memory resided within the PC/AT computer. Likewise, the PC/AT directly controls VME Bus peripherals. The boards pass four of the VME Bus interrupt signals to the PC/AT, which can, in turn, interrupt a VME Bus CPU. $1280.

Bit 3 Computer Corp, 8120 Penn Ave S, Minneapolis, MN 55431. Phone (612) 881-6955. TLX 4997016.

Circle No 403

MODUTEC'S

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THE WORLD'S ONLY LCD DPM WITH SUPER-BRITE LED BACKLIGHTING.

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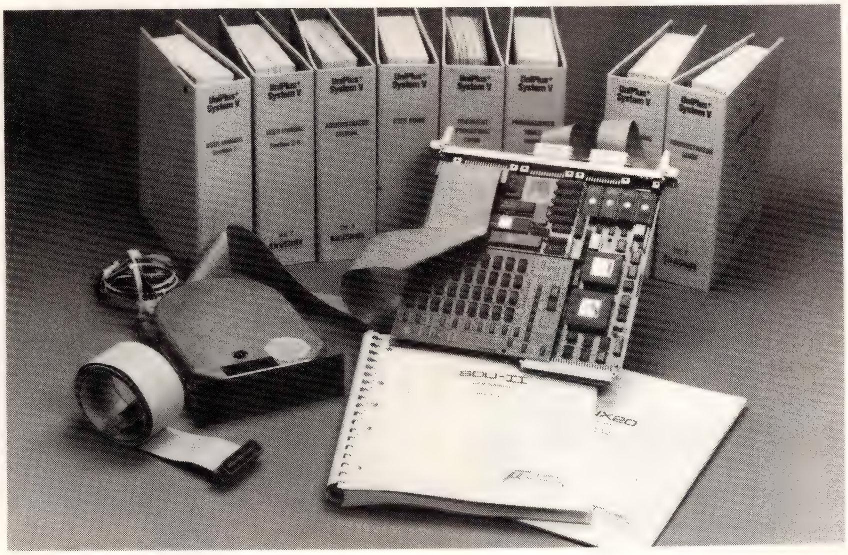
CIRCLE NO 85

INSTRUMENTATION & POWER SOURCES



UNIX DEVELOPER

- *Comes with Unix installed on hard disk*
- *Uses Multibus II backplane*

The SDU-II Unix development system consists of a 68020-based, single-board computer, which plugs into a Multibus II backplane, and a Winchester disk drive. The single-board computer comprises a 16.67-MHz 68020 μP, a 1M-byte RAM (expandable to 4M bytes), a SCSI peripheral interface, and two RS-232C ports. Options include memory-management, floating-point, and I/O expansion modules. The disk drive is available with Unix System V, Release 2, installed. The software includes sample device drivers for several common peripherals and instructions for reconfiguring other user-supplied devices. Including all hardware, software, documentation, and cabling for running the system, but excluding power supply, cabinet, and CRT, the price is $8900.

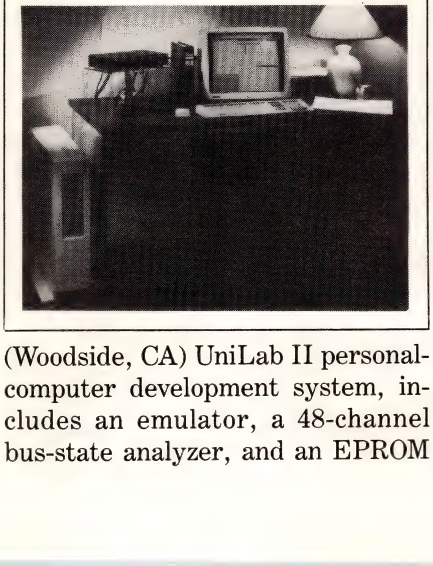
Microbar Systems Inc, 785 Lucerne Dr, Sunnyvale, CA 94086. Phone (408) 720-9300.

Circle No 404

VAX DEVELOPER

- *Windows show source code, traces, menus, and commands*
- *Supports more than 120 μPs*

The Viceteam μP development system works with DEC VAX computers. The instrument supports more than 120 processors, including the 68HC11, the 8096, and the 1750A MIL STD. To retool the device for any of these processors, you need an additional software/cable package. The unit's hardware/software package, based on Orion Instruments'



(Woodside, CA) UniLab II personal-computer development system, includes an emulator, a 48-channel bus-state analyzer, and an EPROM programmer. The software has a windowing system that simultaneously displays source code, real-time event traces, menus, and a list of commands. The windows allow you to control multiple in-circuit emulators from a single terminal. Other standard features include command macros, user-definable keys, a Hex calculator, an on-line assembler, 32k bytes of emulation memory (expandable to 128k bytes), and screen printing via a print spooler. $6500.

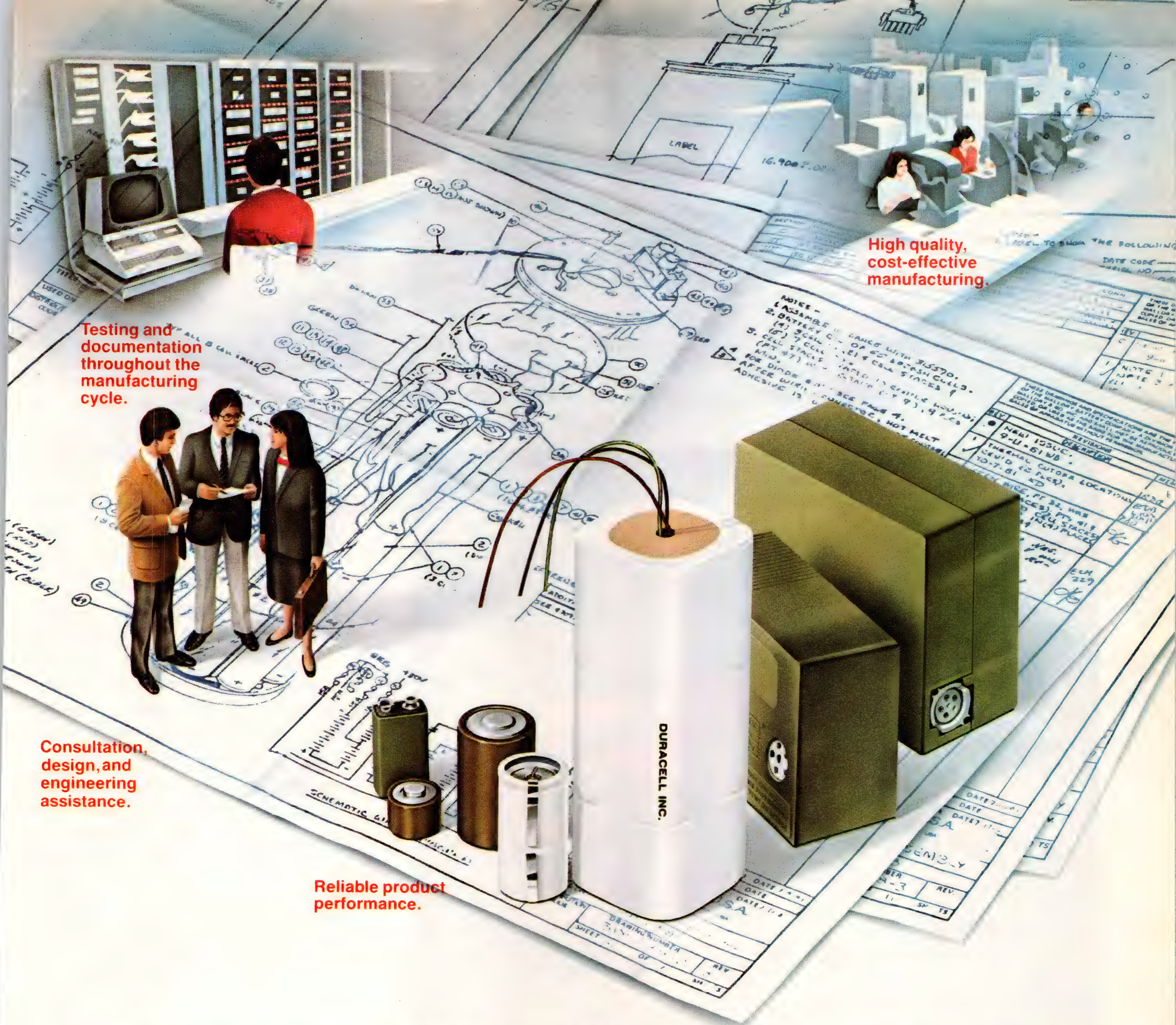
Compu-Mech Inc, 5242 Angola Rd, Toledo, OH 43615. Phone (419) 535-6702. TLX 510-601-7362.

Circle No 405

IC TESTER

- *Tests ICs that have built-in or user-supplied truth tables*
- *Programs EEPROMs*

The Triple Crown 700, a personal-computer-hosted instrument, performs three functions: It tests digital ICs, it programs EPROMs, and it tests memory chips. The unit comes with truth tables for 700 ICs, but you can add your own tables for custom devices. It can program 16k- to 256k-bit EPROMs, and if you add an adapter, it can also program megabit EPROMs. An optional software module allows you to program an EEPROM. In conjunction with a user-supplied test vector, the in-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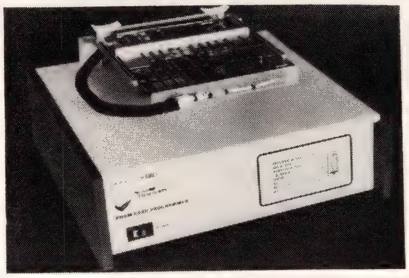
Government Sales & Marketing Group
CIRCLE NO 151

strument can test both static and dynamic RAMs and ROMs. The unit comes with a console, an interface card, diskette software, and an owner's manual. $595.

Computer Service Technology Inc, 717 Lingco Dr, Suite 203, Richardson, TX 75081. Phone (214) 783-9215.

Circle No 406



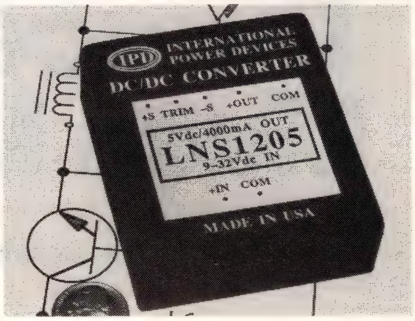
CARD PROGRAMMER

- *Programs PROM arrays on pc boards*
- *Control programs available for the HP85, -9845, -9816, IBM PC*

The PROM Card Programmer programs, reads, and verifies EPROMs, EEPROMs, and programmable single-chip μPs after they have been soldered into a pc board. It can also power a pc board and exercise control of onboard μPs and circuitry, so that you can test components, like RAMs, and burn PROMs. Because the device's programming voltage levels and ports are all configurable by the control program, you can make design changes in a pc board by modifying the command sequence rather than by redesigning of support equipment. Control programs for the HP85, HP9845, and HP9816, and for the IBM PC are available. Programmer, including control software, $11,565; standard pc-board adapters, $250 to $550; custom interface design, less than $5000.

Demo Systems Inc, 19215 Parthenia St, Northridge, CA 91324. Phone (818) 885-6226.

Circle No 407



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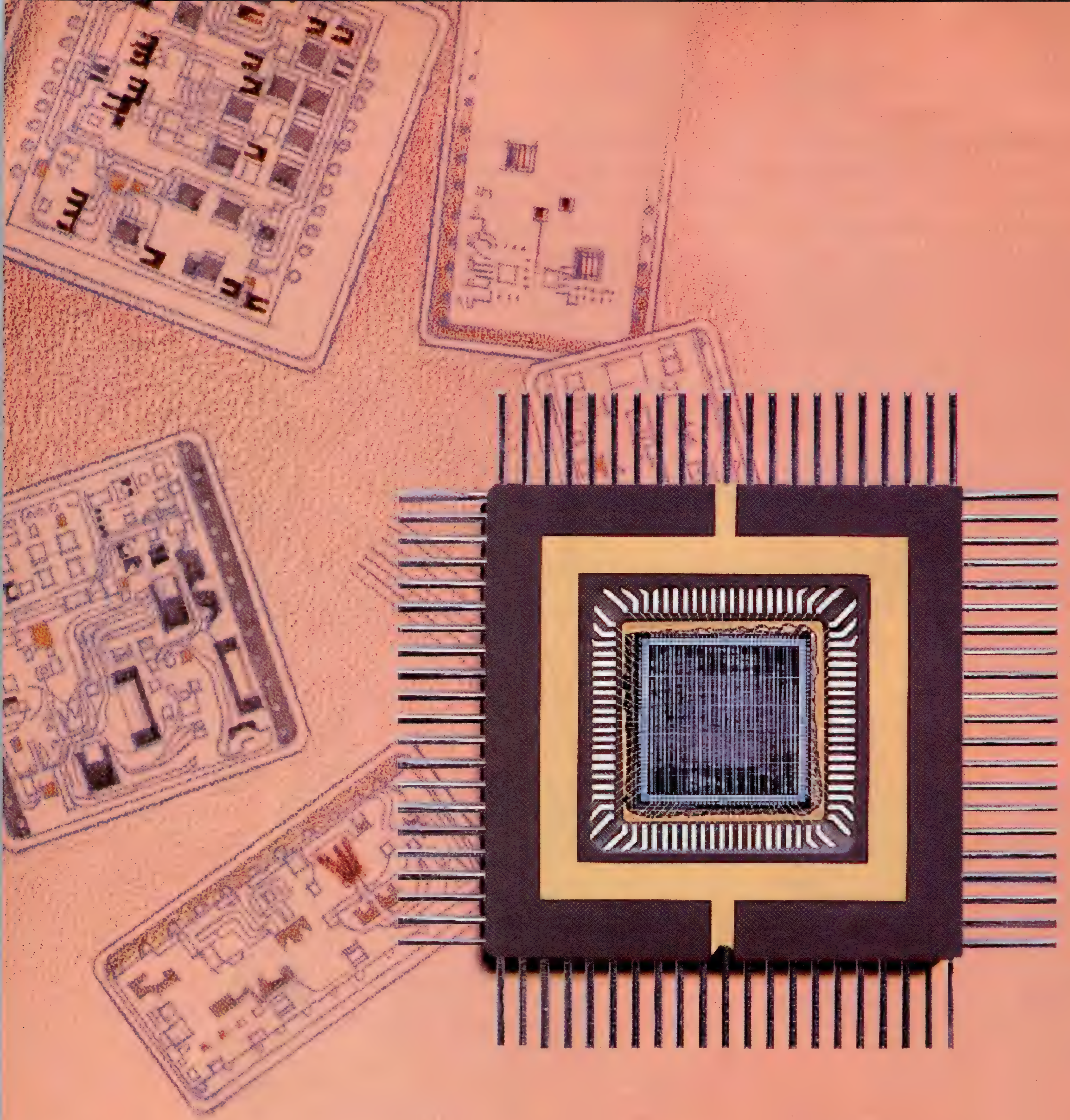

A compact 1553 that carries a busload.

The UT1553B BCRT data bus system proves that big things do come in small packages. It's loaded with features including both MIL-STD-1553B Bus Controller and Remote Terminal functions and advanced, specialized memory management—all on one low-power CMOS chip.

It's the next generation product in our 1553 family. The BCRT was designed to reduce host intervention with automatic DMA and address generation. It automatically executes message transfers, provides interrupts, and generates status information. UTMC's BCRT allows you to implement a pseudo-transparent dual-port RAM configuration.

The BCRT's bus controller uses a linked-list message scheme to provide the host with message "chaining." Memory space is optimized by using programmable address pointers. As an RT, the BCRT implements time tagging and message history functions. It also supports multiple-message buffering—up to 128—including variable-length messages to any subaddress.

The BCRT complies with the standard LAN used for military systems while meeting selected tests in MIL-STD-883C. It is available in 84-pin LCCs, PGAs, or Cerquads.

Don't miss the bus on your 1553 system needs. Call UTMC.

CIRCLE NO 173

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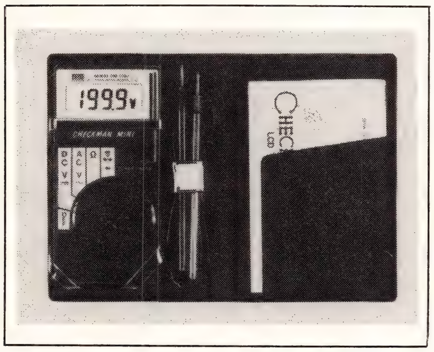
dc for 12V dc output, and 19 to 40V dc for 15V dc output suit battery-operated systems. PWM conversion enables the series to provide ±2% max line and load regulation. The series features ripple and noise of 50 mV p-p or 10 mV rms max at 20-MHz bandwidth. Temperature coefficient is ±0.01%/°C. All models have overvoltage protection. Operating temperature range is −25 to +71°C with no derating. Available outputs are 5, 12, and 15V at 4, 3, and 3A respectively. In a 6-sided case shield, $39 (1000). Delivery, four weeks ARO.

International Power Devices Inc, 155 N Beacon St, Brighton, MA 02135. Phone (617) 782-3331. TLX 650-273-8631.

Circle No 408



POCKET DMM

- *Autoranging unit*
- *Folds to pocket size*

The Checkman Mini, Model DM1000, is a card-size 3½-digit multimeter. The autoranging unit comes in a vinyl case and has attached probes. It folds to 4.5×3×0.5 in. and weighs 3 oz. The unit measures ac/dc voltages from 2 to 450V. It also measures ohms, tests continuity, and performs diode checks. It features 0.7% basic dc accuracy and has a 0.4-in.-high LCD. Ohm ranges are from 2 kΩ to 2 MΩ. The instrument operates from two 1.5V button-cell batteries. $27.95.

Siber Hegner North America Inc, 5 Landmark Sq, Stamford, CT 06901. Phone (800) 221-5749; in CT, (203) 967-4441. TLX 279653.

Circle No 409

GAUSSMETER

- *Custom-formatted LCD*
- *Handheld unit*

The 4048 handheld gaussmeter reads magnetic fields from 0.1G to 20 kG with an accuracy of 2% dc and 2 to 2.5% ac, depending on frequency. The device has a custom-formatted LCD that shows the magnetic-field reading as well as information on all other functions and modes. The meter comes in a pouch with batteries, a transverse probe, a zero-gauss chamber, and a probe-extension cable. $450.

F W Bell Inc, 6120 Hanging Moss Rd, Orlando, FL 32807. Phone (305) 678-6900.

Circle No 410

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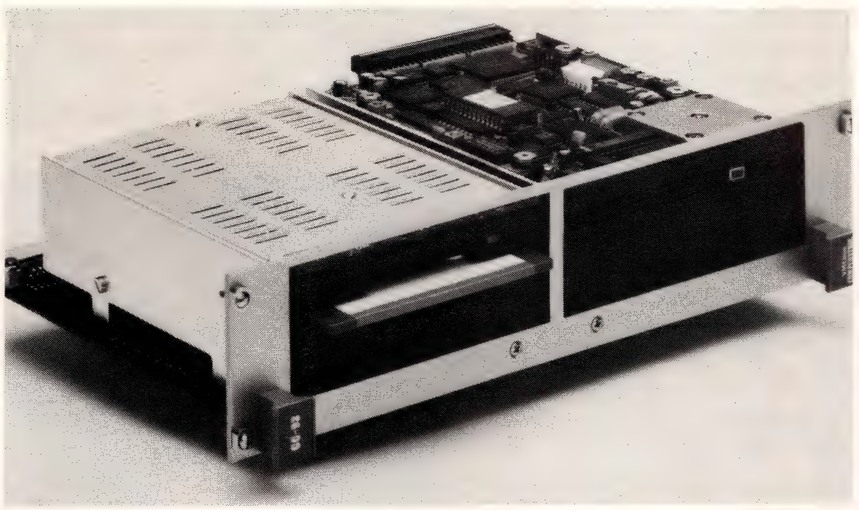

DISK MODULE

- *Has two SCSI bus-compatible 3.5-in. drives*
- *Plugs directly into 6U VME Bus card cage*

The CC-93 is a VME Bus plug-in module that carries two 3.5-in. disk drives. Versions are available with a 1M-byte floppy-disk drive and a 20M- or 40M-byte hard-disk drive, or with two 1M-byte floppy-disk drives. Both drives in the module share a SCSI bus interface, which resides on the VME Bus P2 connector. Each drive has its own SCSI bus ID number, and both logical drives support the SCSI bus disconnect and reselect commands. Power supplies, which typically amount to 2.6A from the 5V supply and 0.8A from the 12V supply, are drawn from the VME Bus P1 connector. Operation spans 10 to 50°C. The 6U module occupies three standard-slot pitches in a VME Bus card cage. Gld 4920 for a module with a 1M-byte floppy-disk and a 20M-byte hard-disk drive; gld 3475 for a module with two 1M-byte floppy-disk drives.

Compcontrol bv, Stratumsedijk 31, 5611 NB Eindhoven, The Netherlands. Phone (040) 124955. TLX 51603.

Circle No 411

Compcontrol Inc, 15466 Los Gatos Blvd, Suite 109-365, Los Gatos, CA 95030. Phone (408) 356-3817. TWX 510-601-2895.

Circle No 412

DRIVER IC

- *Drives 4A stepper motors from supplies to 50V*
- *Has TTL-compatible control inputs*

The IP3D10 4A driver can drive stepper motors or other inductive loads from supplies as high as 50V. It has an H-bridge output stage that includes integral voltage-spike-suppression diodes. The control inputs are compatible with TTL circuitry and have a separate ground pin to improve noise immunity. To reduce power consumption, a separate V_{CC} supply pin allows you to operate the driver's control logic from a 5V supply. Other features of the driver include internal thermal-overload and crossover-current protection. All specifications apply over the full temperature range of 0 to 70°C. The device also has a fully specified reverse-bias safe-operating area. The IP3D10 comes in a 10-pin power SIP or a 9-pin TO-66 package. £3.50 (50,000).

Integrated Power Semiconductors Ltd, MacIntosh Rd, Kirkton Campus, Livingston EH54 7BW, UK. Phone (0506) 416416. TLX 727360.

Circle No 413

Integrated Power Semiconductors, 2727 Walsh Ave, Suite 201, Santa Clara, CA 95051. Phone (408) 727-2772. TLX 350073.

Circle No 414

TRANSISTORS

- *Suit off-line, switching power supplies*
- *One version in an isolated-transistor package*

The 1300V collector-voltage rating of the SGSF425 and SGSIF425 npn transistors eliminates the need for overvoltage-protection snubber circuitry in applications such as color-CRT deflection circuits and off-line switching power supplies. Their $I_{C(SAT)}$ of 1.25A and gain of 5 allow you to use them in 50W flyback-converter or 100W forward-converter switching supplies operating directly from a 240V line (or from a 110V line with an input doubler). The SGSF425 is housed in a SOT-93 (TO-218) plastic package, and the SGSIF425 is housed in an isolated Isowatt-218 package, which conforms to the creepage-distance and isolation requirements of VDE, IEC, and UL specifications. SGSF425, approximately $0.85; SGSIF425, approximately $0.95 (10,000).

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SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100.

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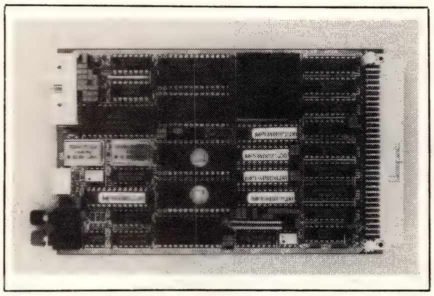


CPU CARD

- *Has an 8-MHz 68000 μP*
- *Features programmable RS-232C interface*

Suiting use with G96 Bus systems, the GESMPU-4B features an 8-MHz 68000 μP and includes four sockets for as much as 256k bytes of ROM or EPROM and 64k bytes of RAM. It also includes a programmable RS-232C interface and a triple counter/timer. The CPU has an 8M-byte addressing range, is I/O address-map compatible with the company's G64 Bus GESMPU-4A CPU card, and runs application software written for the GESMPU-4A. Sw fr 750.

Gespac sa, 3 chemin des Aulx, 1228 Plan-les-Ouates/Geneva, Switzerland. Phone (4122) 713400.

Circle No 417

Gespac Inc, 100 W Hoover Ave, Suite 11, Mesa, AZ 85202. Phone (602) 962-5559.

Circle No 433

CODED SWITCHES

- *Can have BCD or hexadecimal coding*
- *Horizontal or vertical mounting*

The DRS and DRR Series of 10×10-mm, pc-board-mountable rotary switches include versions with BCD or hexadecimal coding and true or complemented outputs. You can also choose versions with a flush actuator, or with a 7-mm-long actuating shaft that incorporates the screwdriver-tip slot at its end. DRS Series switches mount with the actuator perpendicular to the pc board; DRR Series switches mount with actuator parallel to the pc board. The switch contacts are rated to switch 15V/30 mA dc and to carry 50V/100 mA dc. The contacts have a resistance of 100 mΩ max and are rated for more than 20,000 switching operations. BCD version, DM 2.43 (1000).

Knitter-switch, Knitter & Co KG, Postfach 100233, 8011 Baldham/Munich, West Germany. Phone (08106) 4041. TLX 528338.

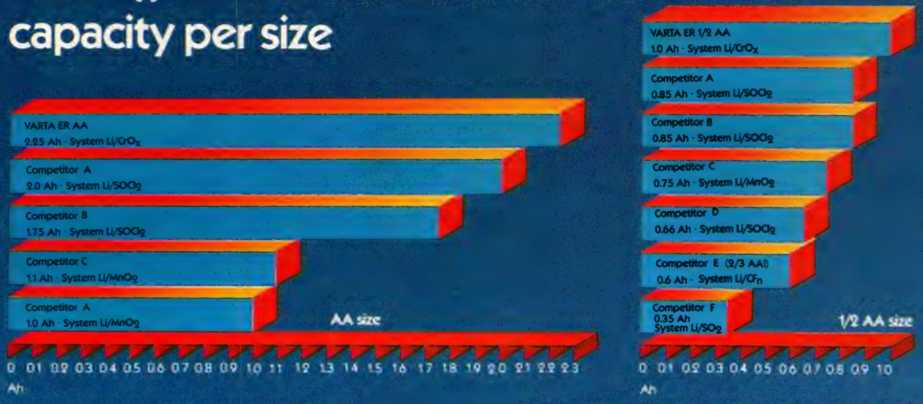
Circle No 418

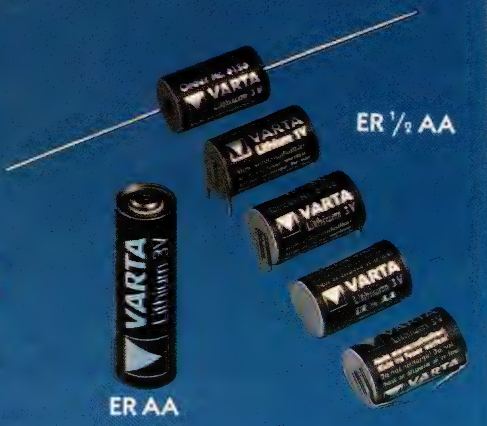
DEVELOPMENT SYSTEM

- *For Hitachi 6301 Series microcontrollers*
- *Based on IBM PC*

The CT6301MDS is an IBM PC-based development system for Hitachi 6301 Series microcontrollers. The system includes a window-based text editor and file-management system, a relocatable macroassembler and linking loader, a symbolic emulator, an EPROM programmer, and an external trace/trigger probe. It supports the

Li/CrO$_x$ – only from VARTA: the battery-system with the highest capacity per size





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VARTA Private Ltd., P.O. Box 55, Bedok North Post Office, Singapore 9146

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CIRCLE NO 177

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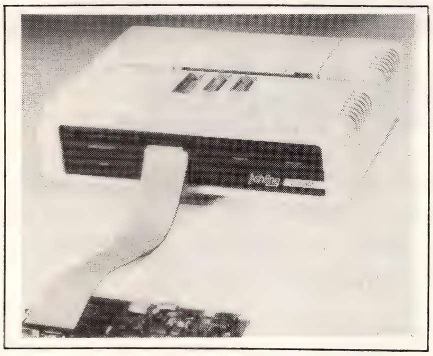
* The products shown here are a brief intro to Tokin's lineup of electronic materials and devices. For a complete picture, be sure to drop by our booth.



HD6301X, -63701X, and -6303X microcontrollers. The EPROM programmer also programs the one-time-programmable, zero-turn-around-time (ZTAT) versions. Adapters are available for the 40-pin HD6303R, and for the HD6301Y, -63701Y, and -6303Y 16k-byte EPROM versions. The in-circuit emulator includes single-step, multiple-step, step-until, and step-while commands, and it allows you to set up as many as 65,536 program-fetch, data-read, or data-write breakpoints. A timer, which monitors program-execution times, allows you to halt the program after a specified period. The emulator also includes a logic-state analyzer with a word width as high as 80 bits, a word depth of 2k bits, and flexible triggering capabilities. $9250.

Ashling Microsystems Ltd, Enterprise House, Plassey Technological Park, Limerick, Ireland. Phone (061) 334466. TLX 70357.

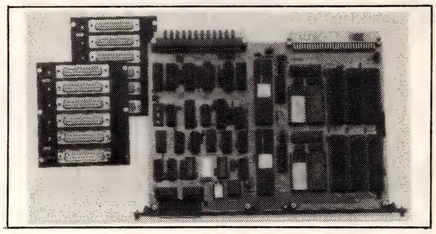
Circle No 419

Ashling Microsystems Inc, 542 Lakeside Dr, Suite 2, Sunnyvale, CA 94086. Phone (408) 720-9131.

Circle No 420

SERIAL I/O CARD

- *12 asynchronous serial I/O channels*
- *Resident firmware manages a 1k-byte data buffer for each channel*



The ISI-1/68K double-Eurocard VME Bus board provides 12 asynchronous serial I/O channels that operate between 50 and 38,400 baud. It also provides sufficient local intelligence to offload most of the serial I/O control tasks from the system's CPU. Resident firmware, running on two 68121 subprocessors, manages a 1k-byte data buffer for each channel, interrupting the host CPU only when the buffer is filled with a certain number of bytes, or when a programmable time-out is exceeded after receiving data bytes. Thus, the host CPU can transfer as many as 108 characters in one interrupt cycle. The firmware allows you to select serial I/O parameters, including stop bits, parity, baud rate, hard-wire hand-

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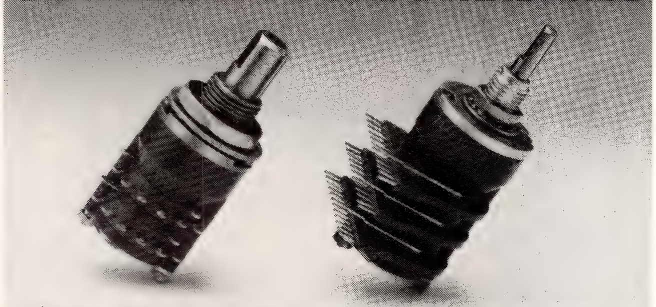

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CIRCLE NO 35

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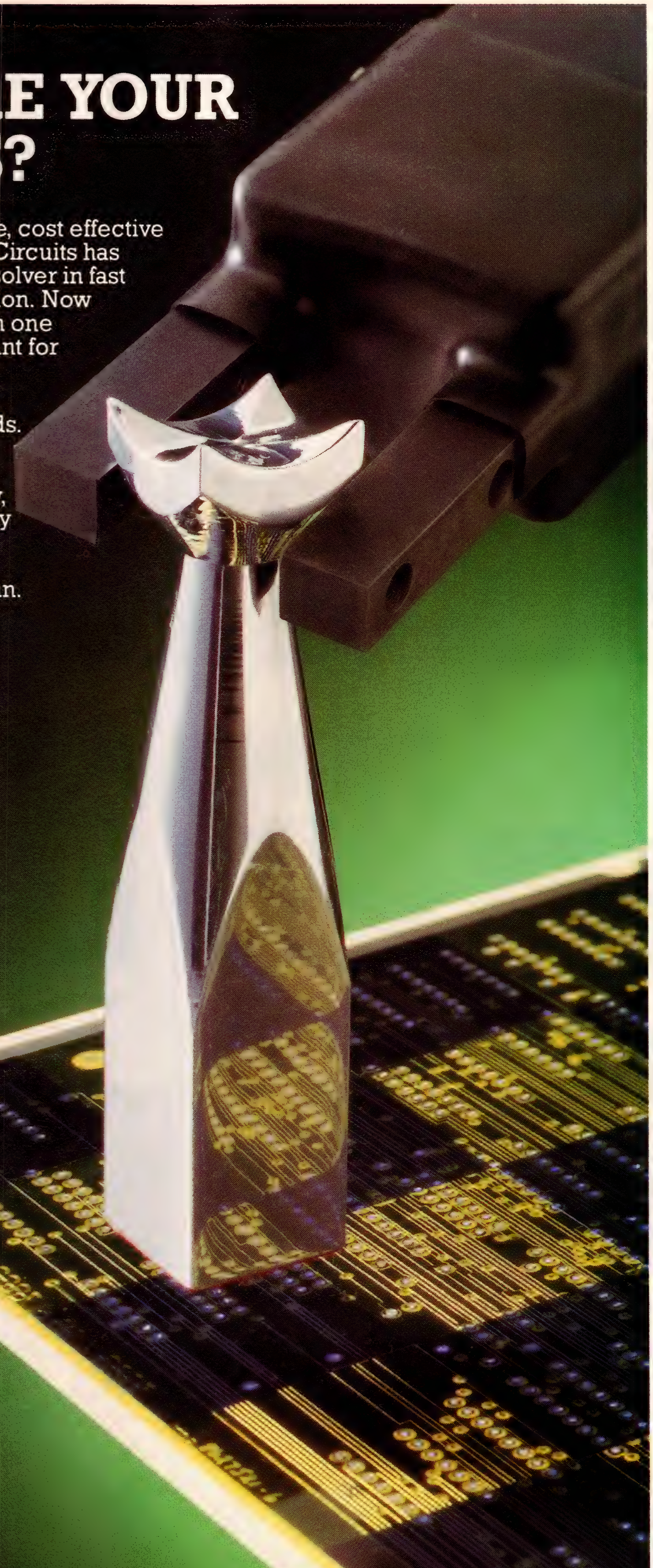

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shaking, and X-On/X-Off characters. It also handles the error protocols necessary when parity-error, over-run, or break-detect conditions occur. A back panel with 12 RS-232C interfaces is standard; RS-422 and current-loop interface back panels are optional. DM 3200.

Eltec Elektronik GmbH, Galileo-Galilei-Strasse 11, 6500 Mainz 42, West Germany. Phone (06131) 50630.

Circle No 421

OSCILLOSCOPE

- *350-MHz, 2-channel unit*
- *Remote-control unit engages front-panel setups*

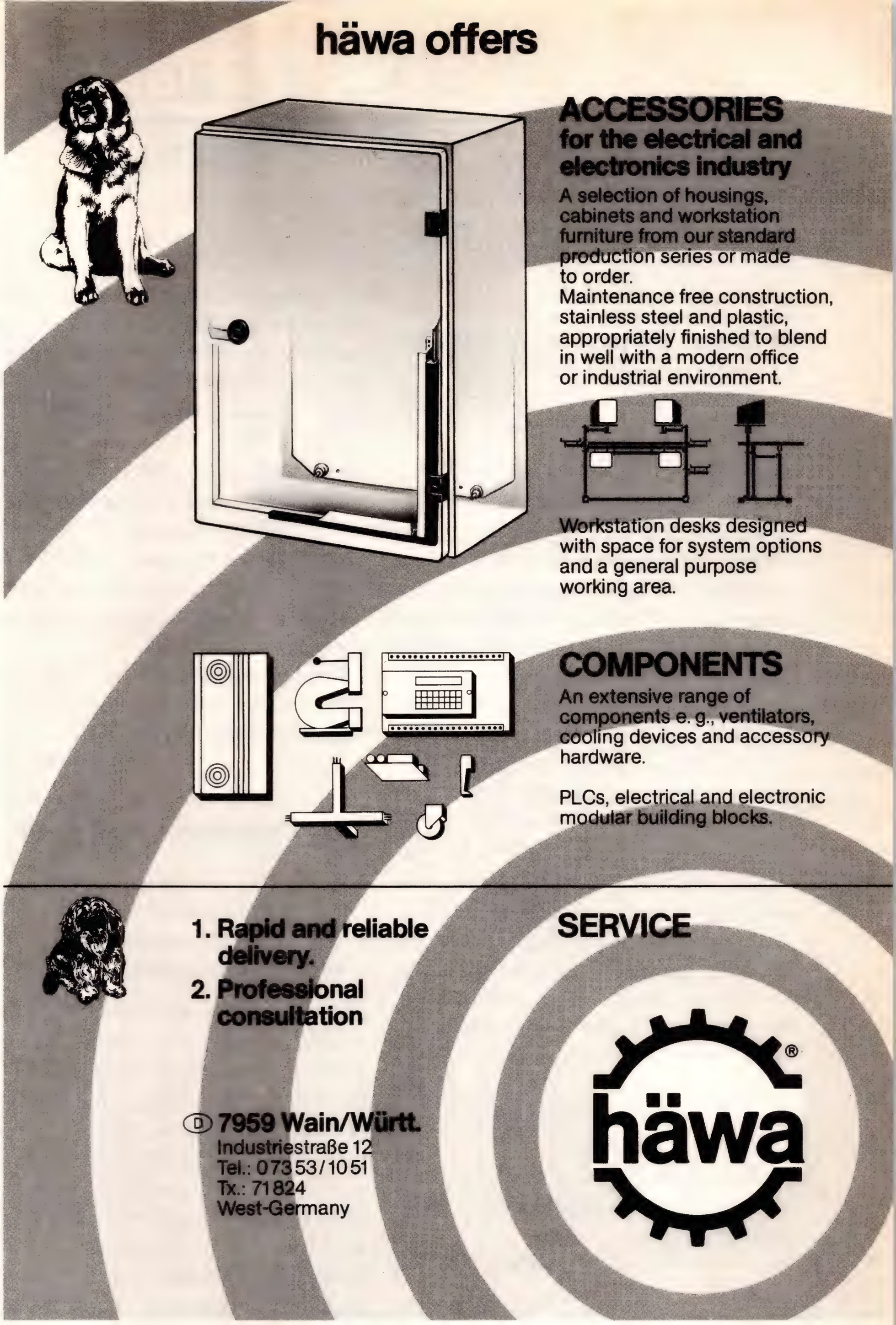
The PM 3296 is a 350-MHz, 2-channel oscilloscope. It features a handheld IR remote-control unit that allows you to choose from as many as 75 different front-panel setups. To select each of the remote-control setups, you first set up the instrument. Pushing the Save button on the remote-control unit stores the instrument setup in the scope's internal memory. You can alter one or all of the scope's front-panel controls between setup-storage events. The handheld unit then allows you to select particular setups, to step forward or backward through setups, or to delete or insert them—a useful feature when direct access to the instrument is either inconvenient or hazardous. You can use the same handheld unit to remotely control several PM 3296s, or you can add an identifier code so that control is unique to one instrument. The measurement capabilities of the PM 3296 are identical to those of the earlier PM 3295. $6500.

Philips, Industrial & Electroacoustic Systems Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 422

Philips Test & Measurement Inc, 85 McKee Dr, Mahwah, NJ 07430. Phone (201) 529-3800.

Circle No 423



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MATH PACKAGE

- *Draws equations using standard mathematical notations*
- *Recalculates results when you change parameter values*

MathCAD is a software tool that helps you enter and modify equations on the screen; you can also create plots and enter or modify explanatory text. Once you enter an equation and specify parameter values, you need only press one key to make the program compute the equation and display the result. The system runs on an IBM PC, PC/XT, or PX/AT, or on a compatible computer running under MS-DOS 2.0 or later versions. The software requires 384k bytes of RAM, a Hercules (Berkeley, CA) monochrome graphics board, and either an IBM Color Graphics Adapter (CGA) or an IBM Enhanced Graphics Adapter (EGA). It can operate with both the Intel 8087 and 80287 coprocessors, the IBM graphics printer, Epson (Torrance, CA) graphics printers, and the Hewlett-Packard laser-jet printer. $189.

MathSoft Inc, 1 Kendall Square, Cambridge, MA 02139. Phone (617) 577-1017.

Circle No 424

FILE SERVER

- *Links networks with as many as four different topologies*
- *Allows print spooling*

The Omniserver is the company's file server using Version 2.0A of Novell's (Orem, UT) Advanced Netware, a universal operating system optimized for use with multiple networks. The system allows interconnection of as many as four different network topologies in the company's file server. It also connects multiple LAN network cards in the file server to increase throughput and thereby increase the number of users. The software allows automatic print spooling and features five menu-driven utilities. These utilities include Session, to manage the network; Filer, to aid in file management; Syscon, an improved version of Novell's system configuration utility; Queue, to help you manage print queues; and Menu, for creating your own menus. Advanced Netware, 8-user version, $850; 100-user version, $1595.

Corvus Systems Inc, 2100 Corvus Dr, San Jose, CA 95124. Phone (408) 559-7000. TLX 278976.

Circle No 425

ELECTROANALYSIS

- *Lets an Apple II control electrochemical measurements*
- *Menu-driven for ease of use*

Mices (microcomputer-controlled electroanalysis system) runs on an Apple II and, in conjunction with the vendor's Adalab data-acquisition interface, automates electrochemical measurements such as cyclic voltammetry, differential-pulse voltammetry, chronocoulometry, and cell resistance. The program is written in machine language to ensure maximum execution speed and allows multiple cyclic voltammetry

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CONVERSION PROGRAM

- *Converts documents from one format to another*
- *Preserves format commands during communication*

Mirrors/PC is a word-processing document- and file-conversion program. It runs on an IBM PC/XT or PC/AT, or on a compatible computer, and it requires 256k bytes of memory and MS-DOS 2.0 or later versions. The program converts MS-DOS files to and from Wordstar, Wordperfect, Multimate, PFS: Write, IBM Writing Assistant, and Volkswriter formats. The program accepts ASCII and EBCDIC (extended binary-coded decimal interchange code) formats for conversion to any of the word-processing packages that the program supports. It allows you to transmit a document over communications lines without using special communications software; this feature preserves formatting and special commands embedded in the document. $149.

Mastersoft Inc, 909 Electric Ave, Suite 202, Seal Beach, CA 90740. Phone (800) 654-5301; in CA, (213) 493-2471.

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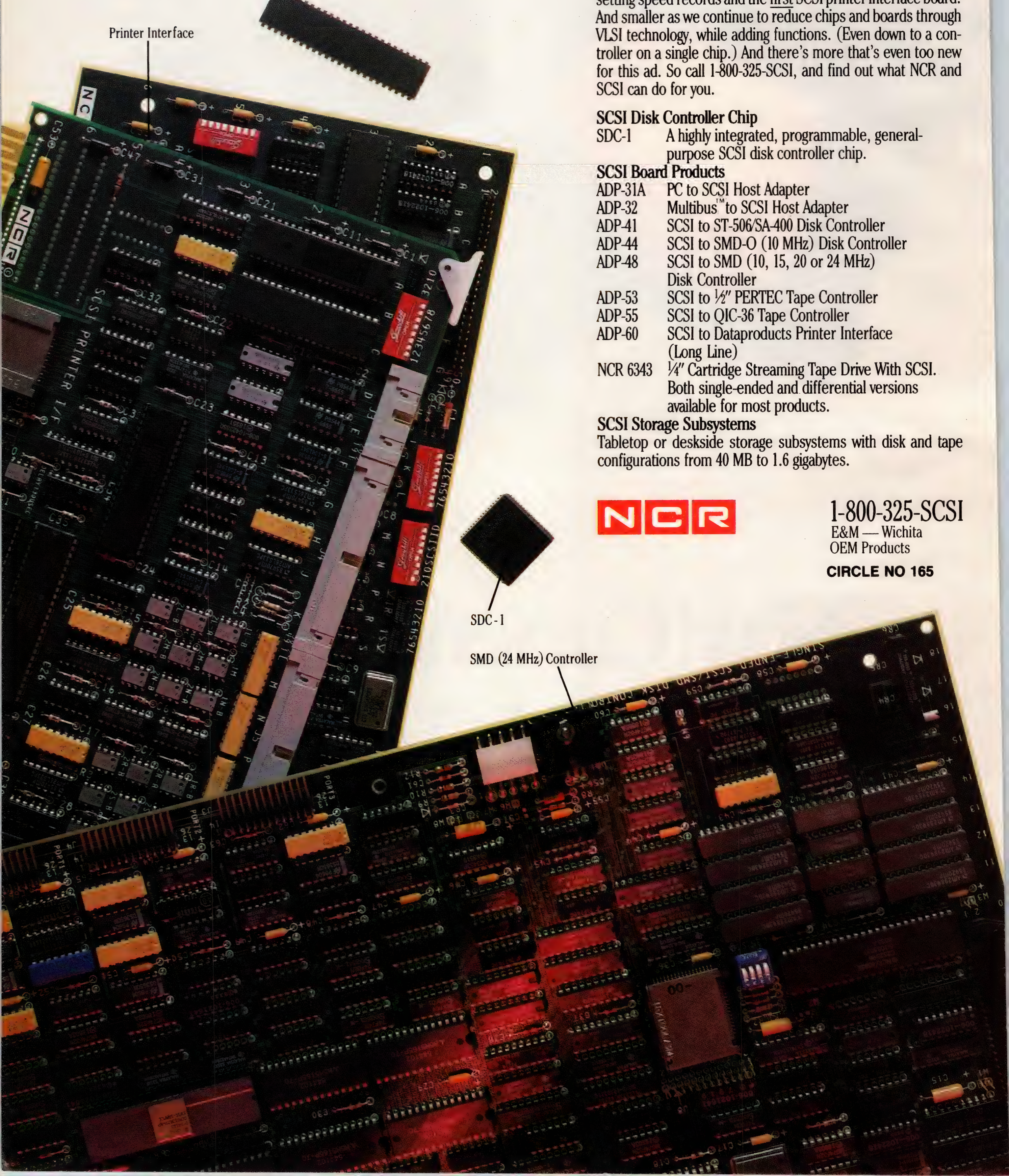

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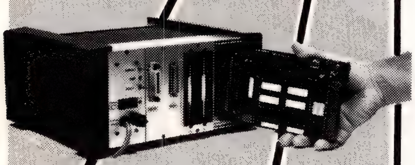

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scans with as many as seven different potential limits. During data collection, the program displays the data on the screen. You can expand any portion of the data to view minute details, and you can send the screen display to a dot-matrix printer or to a plotter. Post-run reports include peak current, peak area, and the slope and intercept for plots of Q vs the square root of time. You can store the collected data on disk for later review. To run the program, you need a 64k-byte Apple II, two disk drives, the Adalab interface, a plotter or graphics printer, and a 3-electrode potentiostat with integrator. $440.

Interactive Microware Inc, Box 139, State College, PA 16804. Phone (814) 238-8294.

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- *Designed for MicroVax systems*
- *Off-line package*

The DIA-MVXII is an off-line memory-diagnostics package for use in MicroVAX II systems. It provides complete diagnostics for all memory arrays down to the chip level; you can also test individual MicroVAX II memory arrays and isolate trouble spots for repair. $750.

EMC Corp, 12 Mercer Rd, Natick, MA 01760. Phone (800) 222-3622; in MA, (617) 655-6600.

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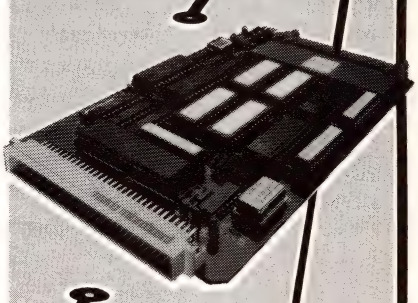
SCIENTIFIC PACKAGE

- *Provides curve-stripping for medical applications*
- *Uses special techniques for least-squares refinement*

Rstrip is a scientific software package for the IBM PC and compatible computers. It's an integrated program for polyexponential curve stripping and parameter optimization in pharmacokinetic analysis and radiologic health applications. In addition to a weighting scheme, the

100% CMOS 68000 INDUSTRIAL COMPUTER



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package includes algorithms that maintain an internal data structure that allows storage of intermediate results. This function eliminates the need to recalculate common functions during recursive stripping. The algorithms included restrict partitioning to those combinations of points that are most likely to include the optimum partitioning and provide for least-squares refinement. The package generates a summary of the statistical analysis; a graphic output is also available. To use the software, you need either a color or a high-resolution graphics adapter, two floppy-disk drives, and 320k bytes of memory. The software is not copy protected. $295.

MicroMath Inc, 3690 E Fort Union Blvd, Salt Lake City, UT 84121. Phone (801) 943-0290.

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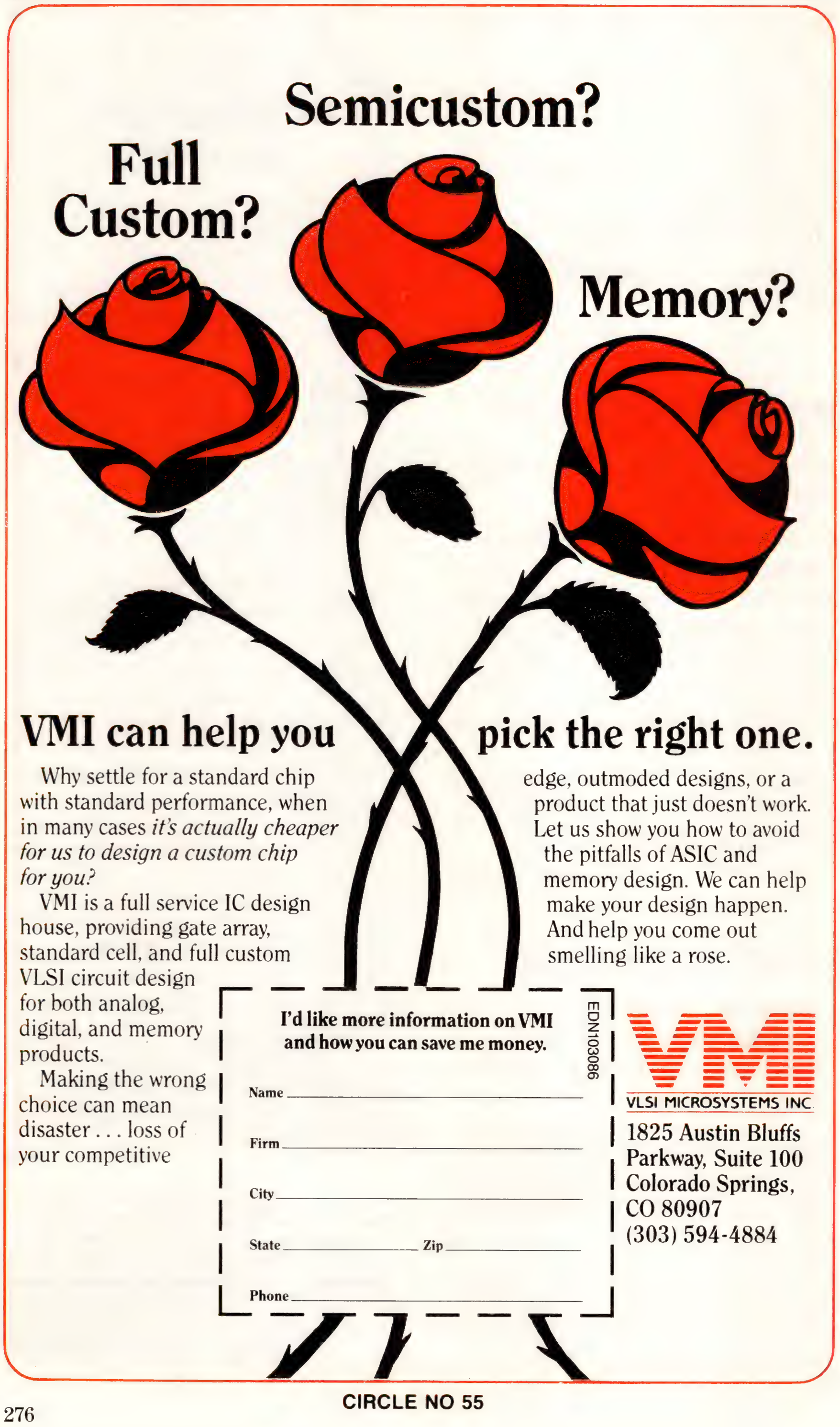
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- *Uses Ward & Mellor and Hatley real-time techniques*

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Index Technology Corp, 101 Main St, Cambridge, MA 02142. Phone (617) 491-2100.

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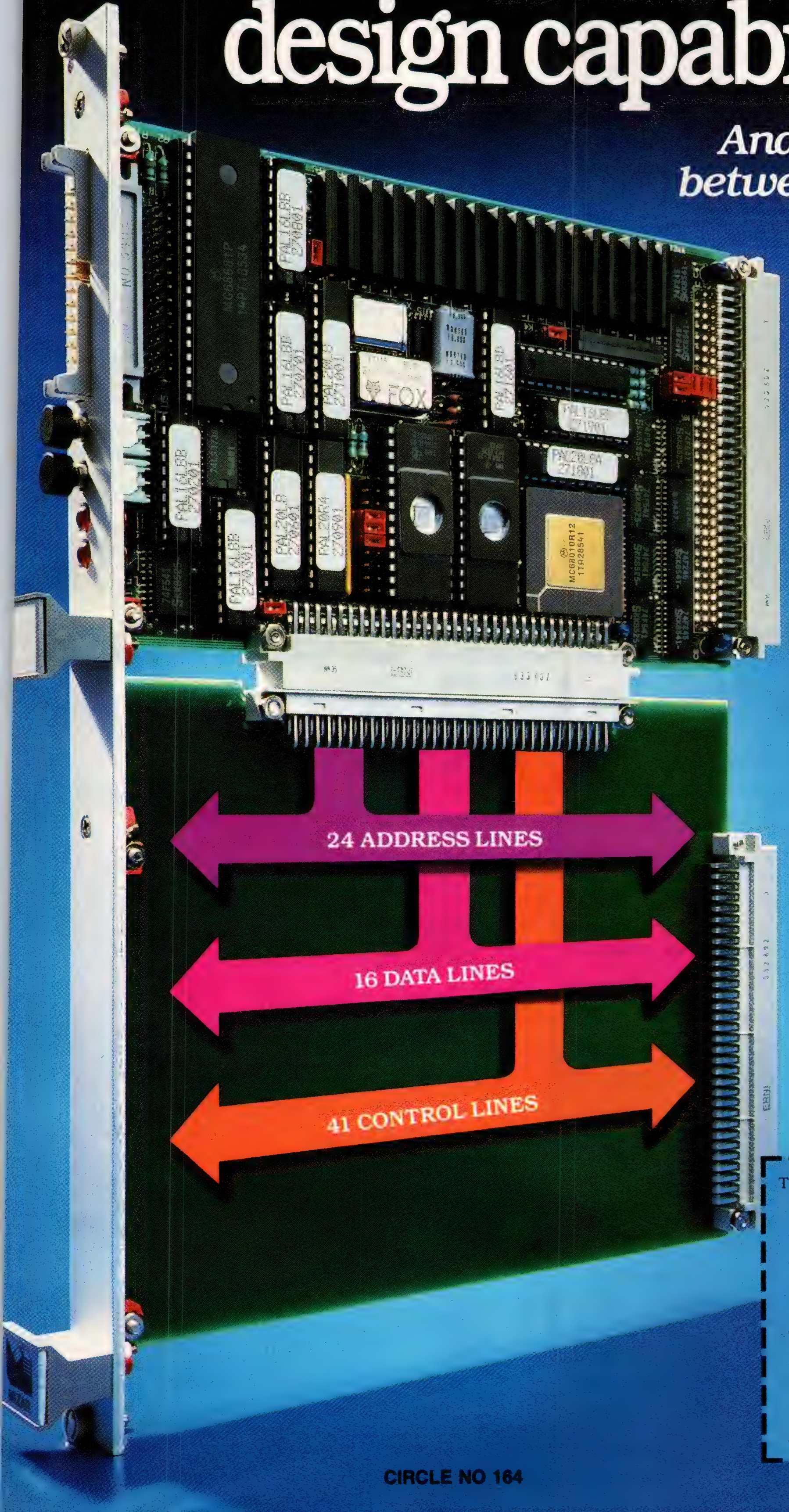

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Both sizes put an enormous amount of information on view . . . an array of 80 characters × 25 lines. But still bulk and power consumption are at a minimum. Battery powered, these slim modules interface with various systems through LCD controller without renewing software.

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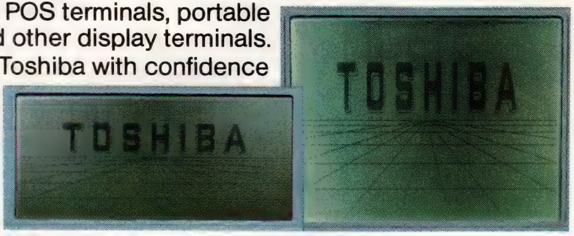
These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.



TLC-363 *TLC-402*

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W × H × D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° ~ 70° C	−20° ~ 70° C
Operating Temperature		0° ~ 50° C	0° ~ 50° C
Supply Voltage	V_{DD}	7 V	7 V
	$V_{DD} - V_{EE}$	20 V	20 V
Input Voltage		$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions			
Supply Voltage	V_{DD}	5±0.25V	5±0.25V
	V_{EE}	−11±3V Var.	−11±3V Var.
Input Voltage	High	V_{DD} − 0.5V min.	V_{DD} − 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

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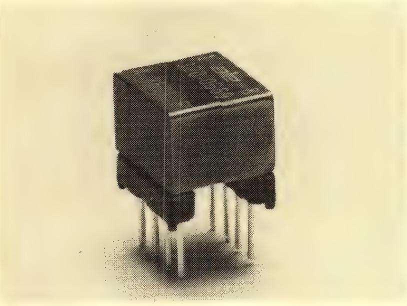

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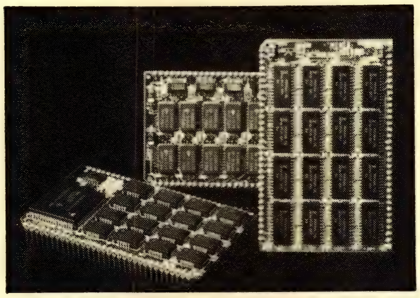

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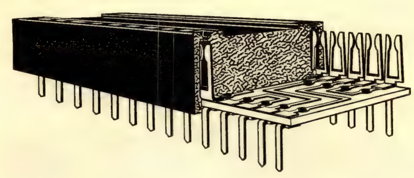

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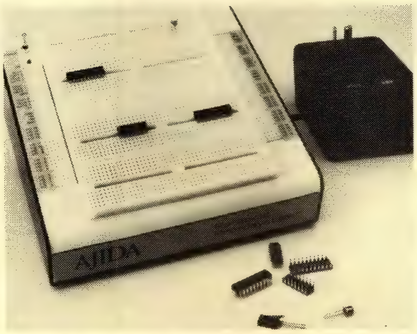

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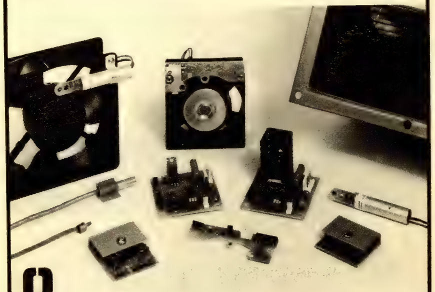

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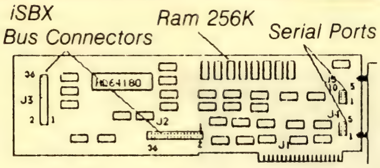

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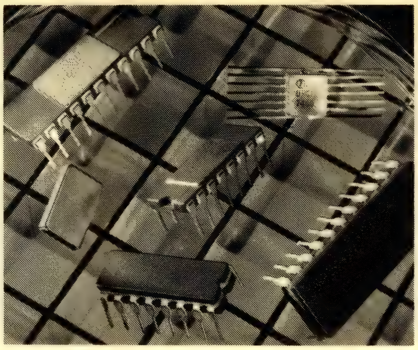

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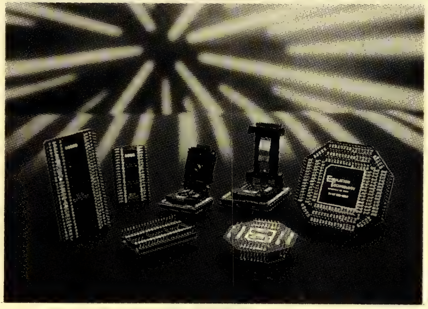

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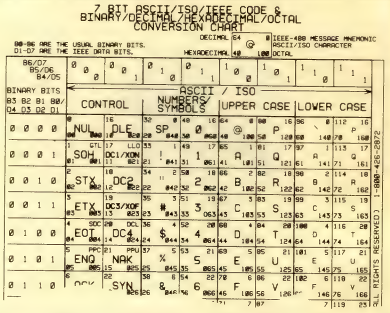

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B6/D7 B5/D6 B4/D5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
BINARY BITS	ASCII / ISO							
B3 B2 B1 B0/ D4 D3 D2 D1	CONTROL		NUMBERS/ SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 00 000	16 DLE 10 020	32 0 SP 20 040	48 16 0 30 060	64 0 @ 40 100	80 16 P 50 120	96 0 ` 60 140	112 16 p 70 160
0 0 0 1	1 GTL SOH 01 001	17 LLO DC1/XON 11 021	33 1 ! 21 041	49 17 1 31 061	65 1 A 41 101	81 17 Q 51 121	97 1 a 61 141	113 17 q 71 161
0 0 1 0	2 STX 02 002	18 DC2 12 022	34 2 " 22 042	50 18 2 32 062	66 2 B 42 102	82 18 R 52 122	98 2 b 62 142	114 18 r 72 162
0 0 1 1	3 ETX 03 003	19 DC3/XOF 13 023	35 3 # 23 043	51 19 3 33 063	67 3 C 43 103	83 19 S 53 123	99 3 c 63 143	115 19 s 73 163
0 1 0 0	4 SDC EOT 04 004	20 DCL DC4 14 024	36 4 $ 24 044	52 20 4 34 064	68 4 D 44 104	84 20 T 54 124	100 4 d 64 144	116 20 t 74 164
0 1 0 1	5 PPC ENQ 05 005	21 PPU NAK 15 025	37 5 % 25 045	53 21 5 35 065	69 5 E 45 105	85 21 U 55 125	101 5 e 65 145	117 21 u 75 165
0 1 1 0	6 ACK	22 SYN 026	38 6 & 26 046	54 22 6 36 066	70 6 F 46 106	86 22 V 56 126	102 6 f 146	118 22 v 76 166
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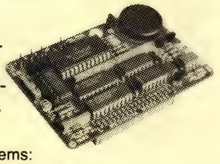

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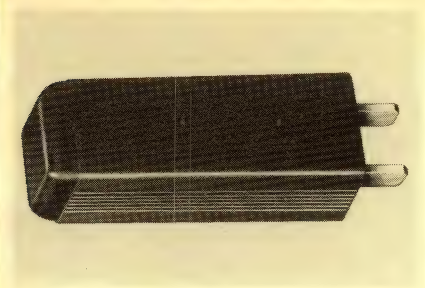

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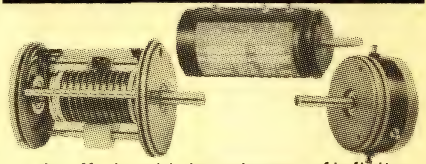

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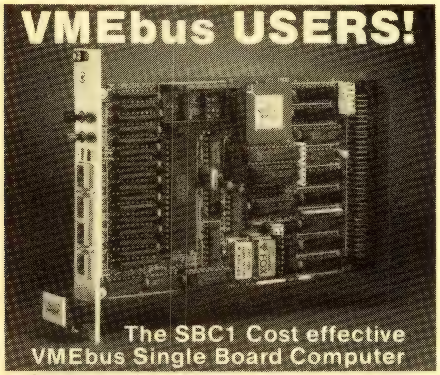

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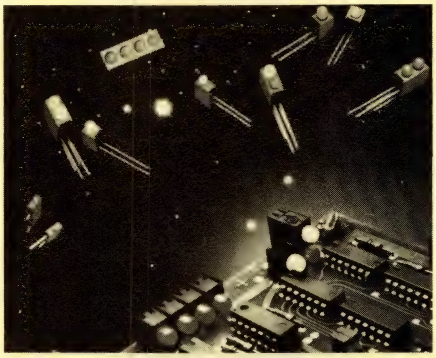

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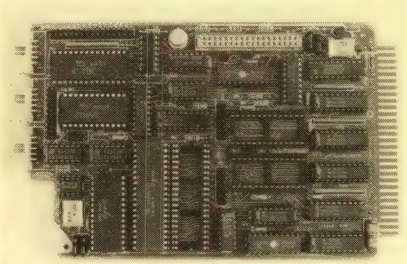

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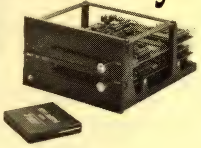

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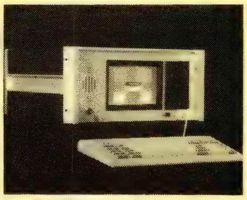

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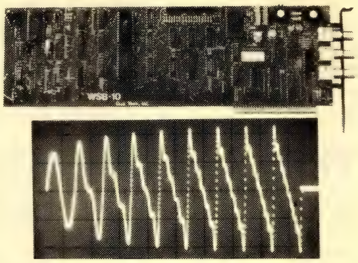

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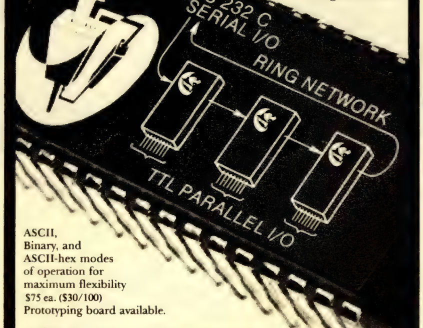

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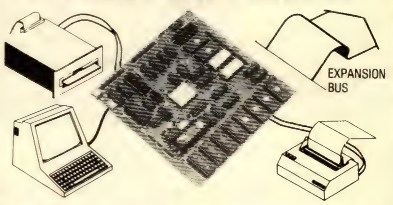

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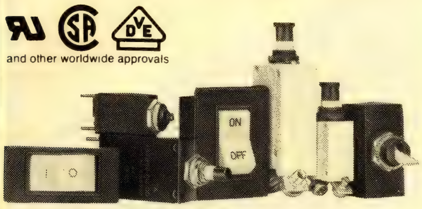

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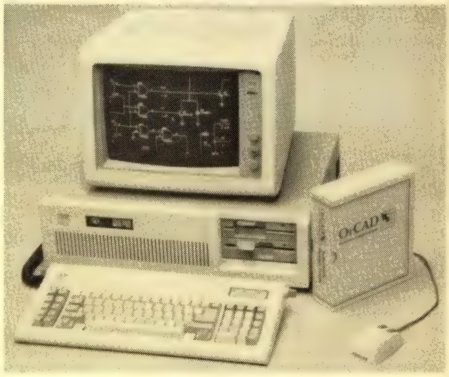

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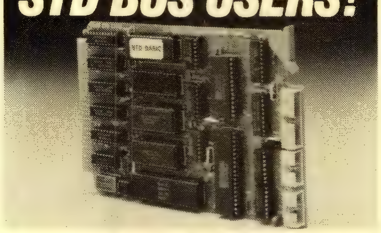

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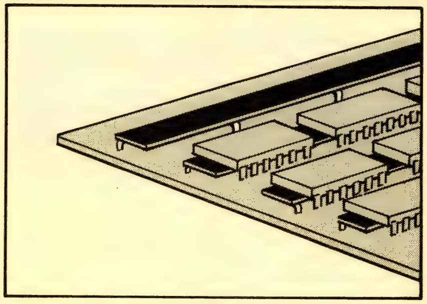

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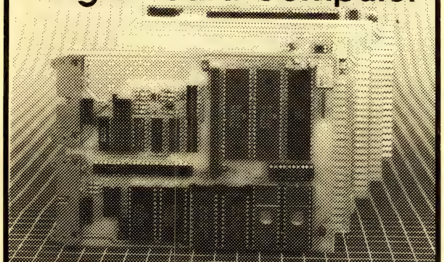

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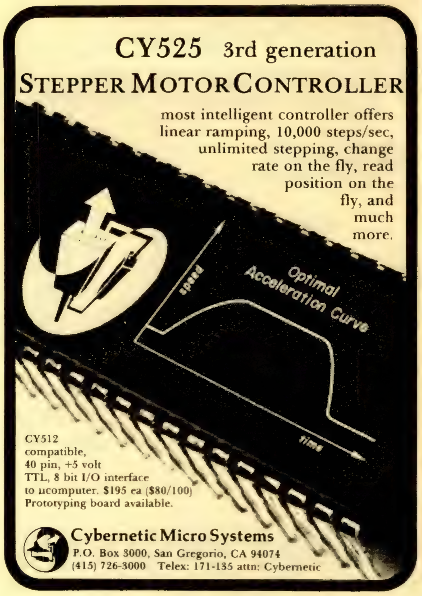

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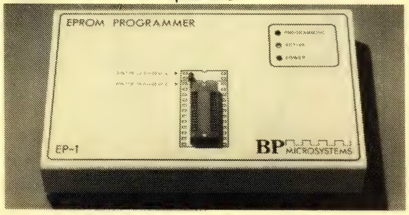

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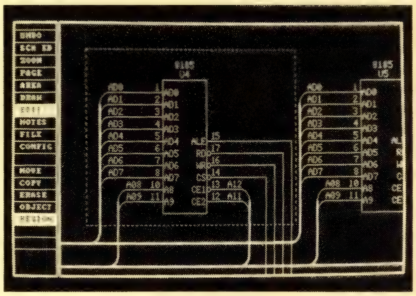

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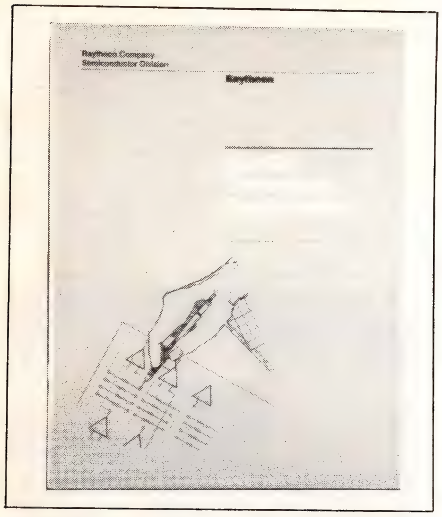

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You can create your own semicustom designs using the information contained in this 56-pg manual. It details the RLA120 linear-array IC, an analog IC that can replace the components an entire pc board would normally hold. A step-by-step process explains how to create a linear-IC schematic from the cells and components in the RLA120. Another section contains data on macrocells and circuit elements; this section is followed by an overview of the design process. Request the manual on company letterhead.

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Manual on data-acquisition measurement

This 76-pg booklet, entitled *How to Make Accurate Low-Level Measurements*, explains various methods of acquiring data from low-level analog sensors. The first chapter describes common sources of analog and digital measurement errors that you might encounter when acquiring data from voltage transducers and thermocouples. The second chapter discusses analog and digital converter designs and techniques, along with their merits and price/performance tradeoffs. The final section covers the company's products, including measurement and control systems for industrial and process application and for wireless monitoring of torque, torsion, and horsepower.

Acurex Corp, Autodata Div, Box 7042, Mountain View, CA 94039.

Circle No 432

Manual helps in surface-mount design

This design manual takes you step by step through the process of surface-mount-technology (SMT) design. A condensed guide, it covers such topics as product selection and analysis, trends in SMT packaging and design, types of SMT assemblies, substrates, and thermal effects. One chapter addresses SMT package specifications and discusses

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CIRCLE NO 57

standards. The book also discusses how to generate designs both manually and with a CAD system. Finally, it includes a set of design rules and a set of instructions for designing a practice SMT board. $350.

Surface Mount Technology Plus, 1786 Technology Dr, San Jose, CA 95110.

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Designer's guide to PC bus

This 144-pg manual is a designer's guide to the PC bus. It defines PC bus-hardware specifications and the BIOS calls required to write software for the bus, as well as pin assignments, signal timing, memory and I/O address maps, electrical requirements, and BIOS interrupt vectors. In addition, the directory covers the company's PC and AT bus products, including brief product overviews, technical information, photos, and diagrams.

Faraday Electronics, 749 N Mary Ave, Sunnyvale, CA 94086.

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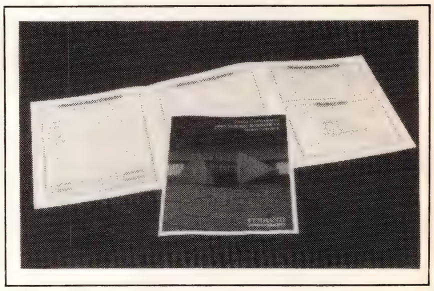

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This short-form brochure highlights the company's line of A/D and D/A converters as well as its line of precision voltage references. The 10-pg guide provides key parameters and packaging options (including surface-mount design) for the monolithic converters and monolithic digital voltmeters. It also presents data on specifications for micropower fixed voltage references, low-power trimmable voltage references, and fixed voltage references.

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LAN books catalogued

This catalog describes 35 books that focus on local-area networks and data communications. The 16-pg pamphlet provides descriptions of books from 15 publishers; for each book, it includes number of pages, table of contents, price, and year of publication. If you fill out the enclosed postcard, you can receive a free LAN glossary by requesting that your name be put on the catalog publisher's mailing list.

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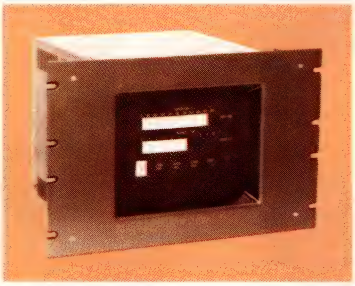

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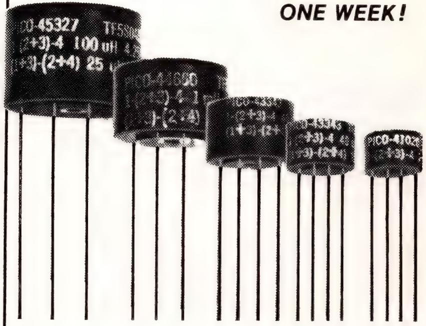

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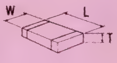
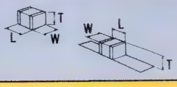
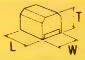
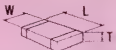
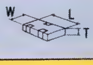
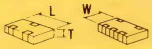
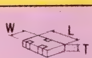
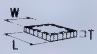
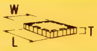
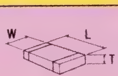
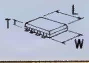
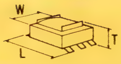
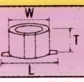
Multilayer Ceramic Chip Capacitor		C1508		1.5	0.8	1.0	C: 0.5 ~ 470pF, 100 ~ 22,000pF
		C2012		2.0	1.25	0.6 0.85 1.25	C: 0.5 ~ 1,800pF C: 470 ~ 100,000pF
		C3216		3.2	1.6	0.6 0.85 1.1	C: 0.5 ~ 270pF C: 470 ~ 220,000pF
		C3225		3.2	2.5	< 1.9	C: 750 ~ 8,200pF, 56,000 ~ 470,000pF
		C4532		4.5	3.2	< 1.9	C: 2,400 ~ 18,000pF, 180,000pF ~ 1μF
		C5650		5.6	5.0	< 1.9	C: 5,100 ~ 33,000pF, 270,000pF ~ 1.5μF
Multilayer Ceramic Chip Capacitor (High Frequency, Los Loss)		FC1414		1.4	1.4	1.6	C: 0.5 ~ 100pF, 150 ~ 3,300pF
		FC2828		2.8	2.8	2.8	C: 0.5 ~ 1,000pF, 470 ~ 22,000pF
		FR1414		1.4	1.4	1.6	C: 0.5 ~ 100pF, 150 ~ 3,300pF
		FR2828		2.8	2.8	2.8	C: 0.5 ~ 1,000pF, 470 ~ 22,000pF
Wound Chip Inductor		NL322522		3.2	2.5	2.2	L: 0.01 ~ 220μH
		NL453232		4.5	3.2	3.2	L: 1.0 ~ 1,000μH
		NLF453232		4.5	3.2	3.2	L: 1.0 ~ 1,000μH
Multilayer Chip Inductor		MLF321606		3.2	1.6	0.6	L:0.047 ~ 220μH
		MLF321611		3.2	1.6	1.1	
		MLF322511		3.2	2.5	1.1	
		MLF322518		3.2	2.5	1.8	
		MLF322525		3.2	2.5	2.5	
Multilayer Chip Transformer		MTT4532		4.5	3.2	2.8 max.	L: 10 ~ 200μH
Multilayer Chip IFT		MIA4532		4.5	3.2	2.8	F:455, 459, 464kHz
		MIF4532		4.5	3.2	2.2	F: 10.7MHz
Multilayer Chip LC Trap		MXT4532		4.5	3.2	2.8 max.	F: fo ±2%
Multilayer Chip LC Filter	HPF (Tuner)	MXF4532H		4.5	3.2	2.8 max.	Electrical characteristics are representative, please specify value when ordering.
	BPF (FM radio)	MXF4532B		4.5	3.2	2.8 max.	
	BPF (VCR)	MXB5050B		5.0	5.0	2.8 max.	
	LPF (VCR)	MXB5050L		5.0	5.0	2.8 max.	
	Equalizer (VCR)	MXB5050E		5.0	5.0	2.8 max.	
	Delay Line (VCR)	MXB5050D		5.0	5.0	2.8 max.	
Multilayer Chip Capacitor Network		MCN7575		7.5	7.5	0.9	C: 1 ~ 1,000pF (TC:CH) (10 capacitors) C:10 ~ 1,000pF (TC:SL) (10 capacitors)
Ferrite Chip Beads		CB201209		2.0	1,25	0.9	Zo: 7, 10, 11Ω
		CB321611		3.2	1.6	1.1	Zo: 19, 26, 31Ω
		CB322513		3.2	2.5	1.3	Zo: 31, 52, 60Ω
		CB453215		4.5	3.2	1.5	Zo: 70, 120, 125Ω
SM Active Delay Line		FDL		12.0	9.5	5.6	Delay time: 20 ~ 250 nsec.
SM Transformer/ Inductor		EE5		7.4	5.3	4.75	Electrical characteristics are representative, please specify value when ordering.
		ER9.5		11.5	9.5	6.3	
		ER11		12.5	11.0	6.3	
		T2		7.0	5.0	2.2	
Step-up Inductor (Piezo Buzzer)		OL3.3×1.6		5.6	5.3	1.6	Inductance values are representative, please specify value when ordering.
		OL3.3×2.1		5.6	3.3	2.1	

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CIRCLE NO 179

A TALE OF TWO START-UPS
PART 1

Opportunities outweigh perils of the market for engineers at fledgling workstation maker

Engineers often give up pleasant work environments and regular hours when they leave established corporations to join start-up companies. In return, they get dingy quarters, long working hours that include nights and weekends, and limited technical support that leaves the engineers with much of the work usually reserved for technicians. But those drawbacks are ancillary, engineers say, to the irresistible challenges that start-ups offer: to explore and apply the latest design technologies, guide a product's development to completion, and work closely with creative and equally motivated people. At one such start-up, Edge Computer Corp, the enthusiasm that goes along with meeting these challenges is pervasive.

The chances of survival for Edge Computer, a young company that entered the workstation market earlier this year, depend on its engineers' ability to match technical wits with their counterparts at such companies as Apollo Computer and Sun Microsystems. Despite the high risk of failure that comes with entering a highly competitive circle of established manufacturers, Edge's 40 engineers, with their first product now on the market, are forging ahead on the design of their next-generation machine.

Like many start-up companies, Edge's origins are rooted in a group of dissatisfied engineers. In 1982, 10 engineers at a division of AB Dick watched as the company's marketing of a minicomputer for office-automation application—a machine the engineers had spent 18 months designing—seemed to falter. After a while, it became apparent that the company would most

Deborah Asbrand, *Staff Editor*

Photographs by James Cowlin

likely abandon its unsuccessful foray into office automation and close the division. Frustrated at the prospect of watching their design—and months of their work—laid to waste, several of the engineers began to talk about forming their own company.

By the summer of 1983, the engineers were meeting in their own homes to discuss their initial idea, a design for an array processor, and to write a business plan. They had hoped to secure venture funding to finance the project, but with none of the group members experienced in management, venture capitalists had little interest in their plan. One venture capitalist, however, had met with three Minneapolis executives who were similarly inclined to strike out on their own. He suggested that the engineers contact the executives about joining forces for a new company.

Part of Edge Computer's engineering team (left to right): Gunnels, Uscinski, Luce, McCarthy, Bernal, Richardson, and Circello.

In July of 1983, one of the executives, Alex Cimochowski, a former vice president of Control Data Corp, flew to Scottsdale, AZ, and met with the engineers in a nearby hotel. Product discussions shifted from an array processor to a workstation. Both parties left the meeting satisfied that they had the makings of a company. On September 19, a date they jokingly refer to as "Black Monday," the 10 engineers submitted their resignations to AB Dick.

Two weeks later, they were at work in a rented hotel conference room, filling out the details of their future machine's architecture on a chalkboard. Ron Bernal, who helped to design and lay out the architecture for the workstation's pipeline processor and now directs advanced product development, still has the seven notebooks full of information he took down at the sessions.

"It was a strange feeling," he says of the company's first few weeks, "but it was invigorating to be working on something that you were really pushing to get done. There were no rules; there were no politics." Weeks later, the group moved to rented quarters in a Scottsdale industrial park. At the new facility, Bernal and the other engineers laid down the carpet and hauled in office desks and chairs. In an area set aside for conferences, a chalkboard rested on the floor, leaning against the wall for support. It remained their main design tool for several weeks.

The sparsely furnished, cavernous area that the company worked out of in its early days was similar to that of many start-ups. Yet despite the prospect of less-than-lush physical settings, small start-up companies hold a strong allure for engineers. Bernal says Edge placed no recruitment advertisements for engineers; the engineers who contacted him about joining the company had all heard news of the venture through word of mouth. The challenge of performing advanced design and the start-up's atmosphere of anticipation were, to the engineers, an unbeatable combination.

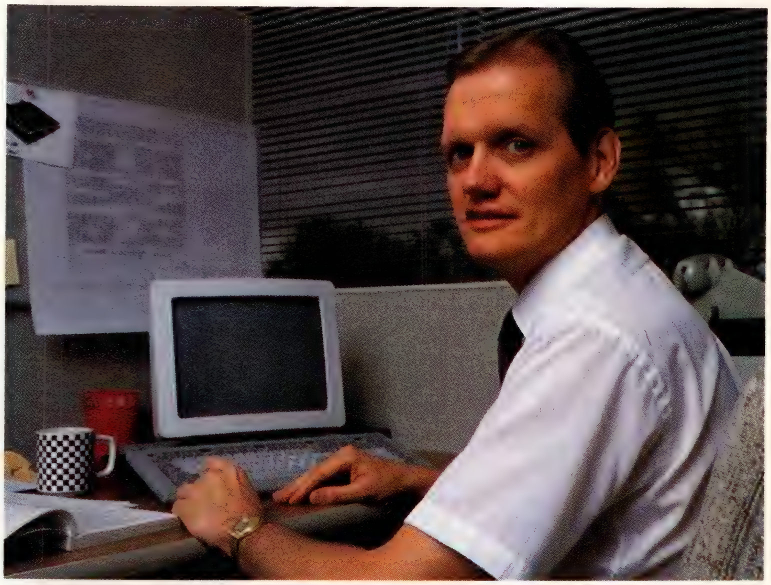
It's not until they join a start-up venture that many engineers are at last assigned to the kinds of design tasks to which they always hoped engineering school would lead them. Roger Luce, one of the original 10 engineers, had held several previous design positions in which he had felt stymied by the lack of challenging design work and the poor leadership under which he worked. At a start-up, he hoped to avoid those impediments.

"I wanted the opportunity to be involved at more levels," Luce says. "I could see where my career path was going to go if I stayed at the other companies. There was no opportunity to be technically innovative, and no product to get excited about." At Edge, Luce's first assignment was the design of the workstation's memory and I/O subsystem using VLSI controller chips.

Many of the engineers at Edge had been frustrated by working at a large company. "The problem with larger companies is that it takes forever to accomplish anything," says Peter Uscinski, a specialist in software development and networking at Edge. "I don't like to spend time waiting for things to happen." Large companies make "too many decisions behind closed doors," says Edge software programmer George Gunnels. "Engineers aren't involved." At large companies for which he had worked, Gunnels says, company politics even entered into the writing of several lines of code.

Joe Circello, too, had grown tired of what he calls the "politicking and bureaucracy" of a large company. Yet that was not the main factor in his decision to join Edge in the winter of 1983. Circello, a hardware designer, had begun looking for a new job when his employer, Honeywell, announced it was phasing out the large-systems division in which he worked. His decision to join Edge, he says, "was strictly a matter of timing." He met with several members of the engineering staff and, finding the chemistry right, went to work for the company in early 1984. "To me it was a no-lose situation," he says. "Even if Edge failed, the experience would have been invaluable."

Indeed, the personal risk of working for a venture-backed start-up company —both in terms of financial sacrifices and career options—is almost nil. To attract top engineering talent to their companies, company founders have to offer competitive salaries and benefits. Edge's engineers received salary offers comparable to what they were earning and they all received stock options. Should the company become successful, the engineers stand to profit from their option to buy shares. The only risk they incurred by joining Edge was that, if the company failed, they'd once again be looking for a job.



Roger Luce, project leader: At other companies, "there was no opportunity to be technically innovative, and no product to get excited about."

Yet market instability attends the electronics industry in all areas. Even large, established companies offer engineers little protection from economic mood swings, says Uscinski. Large companies' habits of cancelling projects when the economy dips, he says, put them on the same par as a start-up company in terms of stability.

For most engineers, the opportunity to do advanced design greatly outweighs any worry of suddenly finding themselves in the job market once again. Designing on silicon and learning more about Unix were enough of an enticement for Dan McCarthy to cancel out any concern he might have had about going to work for a start-up company. "The job was right up my alley," says McCarthy, a hardware designer who worked for Honeywell's large-systems division before it closed. Edge's venture backing further bolstered his decision to accept the company's job offer: "This wasn't a pipe dream; it was for real."

By mid-1984, the company's technical staff was complete. The confluence of engineers and technical challenge formed a company that, in its earliest stages, was an engineer's dream. "Originally, it was just an engineering company; there were no sales and marketing reps," Gunnels says nostalgically. The engineers had set their own ambitious timetable for their product—two and a half years to design, manufacture, and market an engineering workstation. In this case, the engineers' relatively young ages—under 35 in most cases—was probably an advantage, Bernal muses, because no one fully understood, and thus was not daunted by, the magnitude of the project they were undertaking.

Joe Circello, hardware designer: "Even if Edge failed, the experience would have been invaluable."

"In a small company, you shoot for your goals not knowing all the answers; you depend on blind faith and innovation," says Bernal. "Experience hurts you in some ways because people will say, 'That can't be done.'" When McCarthy and Circello, who had been working on one project that extended over several years at Honeywell, first saw the workstation's design schedule, Bernal says, "they thought we were crazy."

Involvement with more than just the technical side of the company's activities was a benefit to many of the engineers. "Early on, I liked [the engineers'] high visibility in the company," says Circello, who describes his meetings with investors and potential customers as informative for him as well as for them. "You become more attuned to the reality of meeting deadlines."

Nick Richardson, who designs floating-point processors at Edge, says that working in a small start-up company lets him see the whole spectrum of a product's development, a view that he missed while working for other employers. "Working for a large company is like working in an ivory tower," he says. "You design something and then two years later you see it on the market."

The stock options that are part of the engineers' compensation package give them a financial stake in the company's future, and, not surprisingly, affect their attitude towards their work as well. Uscinski says that on those Saturdays when he would prefer to stay home, he remembers his own potential financial gain if the product and company becomes successful. Such contemplation is typically short lived, he reports, and he soon finds himself in his office.

Indeed, long hours are a big part of working for a start-up company, and they can impose a hardship. In the company's early days, the workload was often 65 to 70 hours each week. Luce says he typically worked from 8 AM to 7:30 PM and recalls the strain these hours placed on him and his family. The days are shorter now, but they still often add up to 50 hours or more each week. One engineer manages his heavy schedule by arriving at the company each day at 5 AM so that he can leave by 5 or 6 PM and spend time with his family.

The issues of flexibility and long hours were discussed with each job candidate during the hiring process, says Bernal. "You want to make sure they're aware of the personal sacrifices they're going to have to make, because it could have an affect on their home lives. Some people say you can work at a start-up and still keep your family number one, but there are times when you have to walk the line on that." And such a conflict can take its toll in mental energy. "Do you ever wonder whether it's all worth it?" one engineer was asked. "All the time," he replied.

Not every engineer can work at the pace required. Bernal recalls that one engineer quit two days after he started, overwhelmed by the task before him. "We sat down and I talked with him," Bernal recalls. "I was confident he could do the job, but he said no, he couldn't do it. It just totally overwhelmed him."

Despite its tender age, Edge is beginning to show signs of the growing pains that plague more mature companies. For example, as the company begins the design of its next generation of products, Bernal is responsible for assigning engineers either to a support function for existing products or to development of the new ones. He faces the same challenge that perplexes many engineering managers: how to keep engineers assigned to jobs that make the best use of their design strengths. As an engineer, Bernal sympathizes with individuals' disappointment when they aren't given the assignments they want and think they deserve; as a manager, he must find ways to minimize the disappointment and to keep the staff technically creative.

As another sign of its development, Edge recently traded its scruffy, rough-around-the-edges look for a spiffier one. Housed in its new quarters in an industrial park, Edge Computer looks like anything but a start-up company. A receptionist at a modular, metallic desk in a quiet lobby greets visitors. A contemporary mauve and pale-gray color scheme gives the interior the trendy look of a company that wants you to believe it's on the inside track.

It's hard not to get caught up in the enthusiasm of a company that is designing products for a changing, dynamic market sector. It's hard not to be excited by people who obviously enjoy their work, who relish the opportunity to build a new company, and who regard their competition as more perceived than real. Yet there is no escaping the fact that Edge's founders chose to enter a market that is fraught with competition from established industry heavyweights like Apollo, Digital Equipment Corp, and Sun Microsystems. More than ever, Edge's team of engineers has to produce a winning product.

Ron Bernal, director of advanced product development: "In a small company, you shoot for your goals not knowing all the answers."

The company introduced its engineering workstation last spring. The workstation, an expensive, high-performance system, still offered technological and price/performance advantages over competitors' products at the time. Since then, however, Apollo Computer and Sun Microsystems have introduced equally powerful products that some industry watchers say have eroded any advantage Edge's early introduction might have gained for the company.

"Edge suffers from not being a recognized name, and its performance edge has been eroded," says Charles Foundyller, president of Daratech, a Cambridge, MA-based market-research firm. "Consequently, it's going to be rough for them." The company has garnered $17.4 million in two rounds of private financing and hopes to raise more money in a third round this fall.

Some small companies will make it in the workstation market, and their success will be based on the right combination of business skill, technical wizardry, and luck. It might be Edge, but, then again, it might not. **EDN**

Part 2 of this series will profile a start-up company that manufactures boards and was financed entirely by the engineers who work for the company.

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Dec. 11	Nov. 18	Product Showcase—Volume I; ICs & Semiconductors; Hardware & Interconnection Devices; Power Supplies/Sources; Software; Literature on Computers & Peripherals, Components, Test & Measurement Instruments, International Products	
Dec. 25	Dec. 4	Product Showcase—Volume II; Computers & Peripherals; Components; Test & Measurement Instruments; International Products; Literature on ICs & Semiconductors, Hardware & Interconnection Devices, Power Supplies/Sources, Software	

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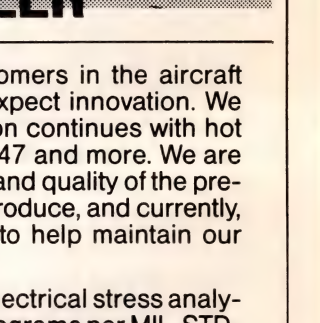

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LOOKING AHEAD

EDITED BY GEORGE STUBBS

HIGH-PERFORMANCE COMPUTERS AND PARALLEL-PROCESSING SEGMENT

(1990)

	TOTAL UNITS	TOTAL DOLLAR VALUE*	PARALLEL-PROCESSING UNITS	DOLLAR VALUE*
SUPERCOMPUTERS	250	$1750	220	$1360
MINISUPERCOMPUTERS	830	$475	700	$405
DATABASE PROCESSORS	1350	$245	1020	$205
ARRAY PROCESSORS	4400	$300	4040	$210
SYMBOL PROCESSORS	4350	$350	3900	$240
SUPERMINICOMPUTERS	44,900	$11,850	17,800	$5600
MAINFRAMES	4000	$24,600	1200	$10,900
TOTAL	60,080	$39,570	28,880	$18,920

*DOLLAR FIGURES ARE IN MILLIONS *(SOURCE: ELECTRONIC TREND PUBLICATIONS)*

High-performance computers to be worth $39.6B in 1990

The quest for greater processing power will lead to widespread use of new, high-performance computers—particularly those employing parallel-processing architectures. The worldwide market for high-performance computers (ie, a machine 10 to 100 times faster than its predecessors in a given category) will grow from $20 billion in 1985 to approximately $39.6 billion in 1990, according to Electronic Trend Publications (Saratoga, CA), publishers of reports on the electronics industry. During those years, the percentage of these machines that are based on parallel processing will grow from 22 to 48%.

Applications of parallel design will be most pervasive in the superminicomputer and mainframe computer categories, representing 87% of the dollar value of systems shipped in 1990. Even so, other, new types of computers—database processors, minisupercomputers, array processors, and symbol processors—will make growing demands on the talents of design experts in parallel processing. This aggregate segment should constitute a $1 billion market by 1990.

The need for faster processing in the scientific and technical fields is not the only factor driving the rapid growth of parallel processing, reports ETP. Single-processor systems are nearing the limits of their capabilities, and today's general-purpose minicomputers and mainframes are not well suited to typical high-performance applications. Also, existing I/O links to application-limited array processors and to networked systems are slow.

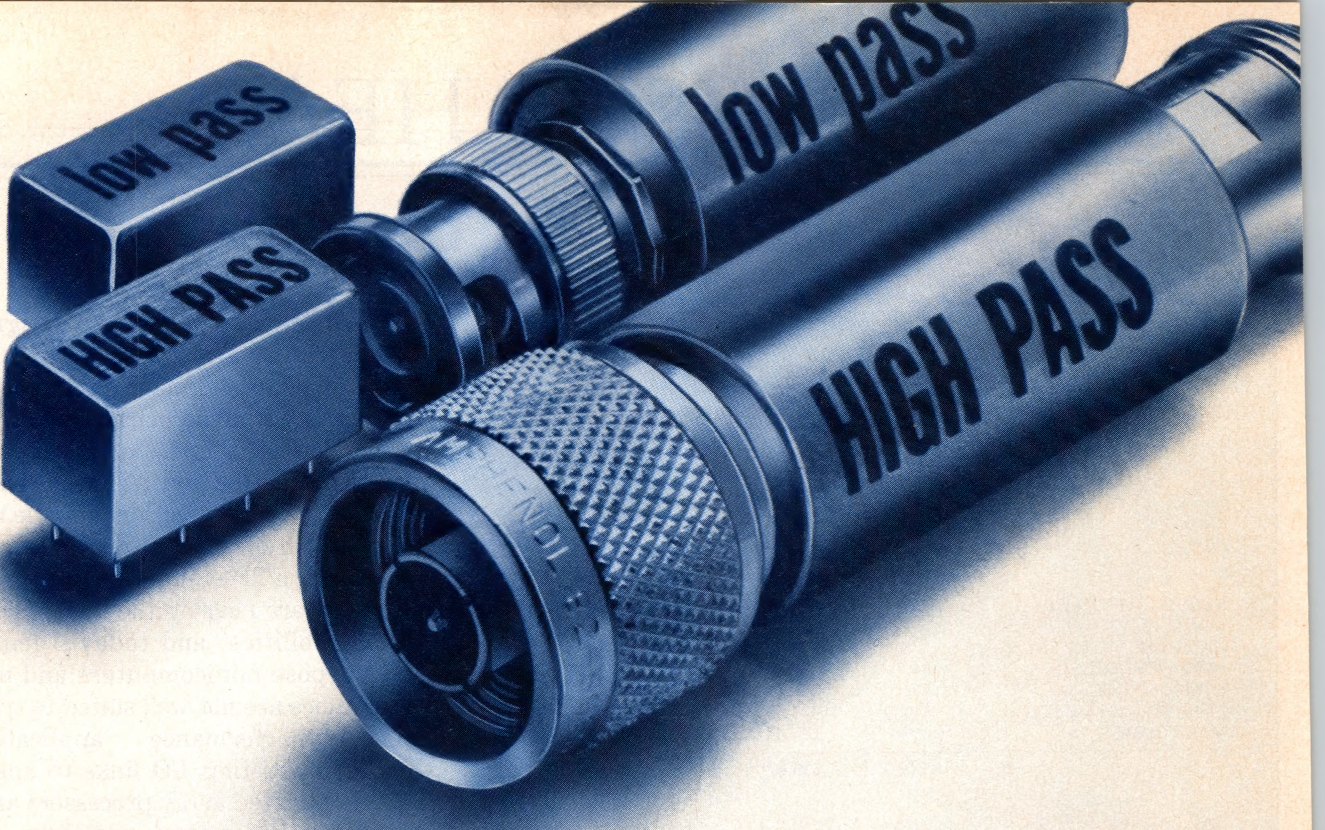
The advance of parallel processing depends to some extent on developments in other areas, such as VLSI circuitry, gallium arsenide ICs, megabit memory chips, faster internal channel speeds, hybrid optoelectronic circuitry, and advanced cooling technology. The principal roadblock to widespread use of parallel-processing architectures is software development. It takes some programming expertise, and some revision of traditional programming styles, to develop operating systems and application programs that can take maximum advantage of parallel-processing architectures.

Multilayer types lead growth in market for pc boards

The market for pc boards will be worth $6.5 billion in 1990, and perhaps as much as $11 billion a decade from now, according to the market-research company Frost & Sullivan Inc of New York, NY. At least until 1990, the fastest growing segment of the industry will be multilayer boards, which will show annual growth rates ranging from 12 to 19% during that time. The pc-board market overall will increase at an average annual rate of 11%.

Multilayer boards contain anywhere from three to more than 20 conductive or grounding layers; therefore, they can support VLSI circuits and reduce the required size of pc-board real estate. Between 1982 and 1985, the market for pc boards of this type doubled. They currently cost $150 to $600 per board.

The less-expensive double-sided boards ($2 to $6 per unit) are still the workhorses of the industry, says Frost & Sullivan, and the market for them is expected to grow at the same rate as the overall market. Flexible circuit boards, accounting for less than 10% of total pc-board sales and costing as much as $20 per unit, are also expected to grow at rates near the total market average. Single-sided pc boards will lose their share of the market, as sales of these simple devices increase by only a 3% average annual rate over the next few years.



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	end, min.	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
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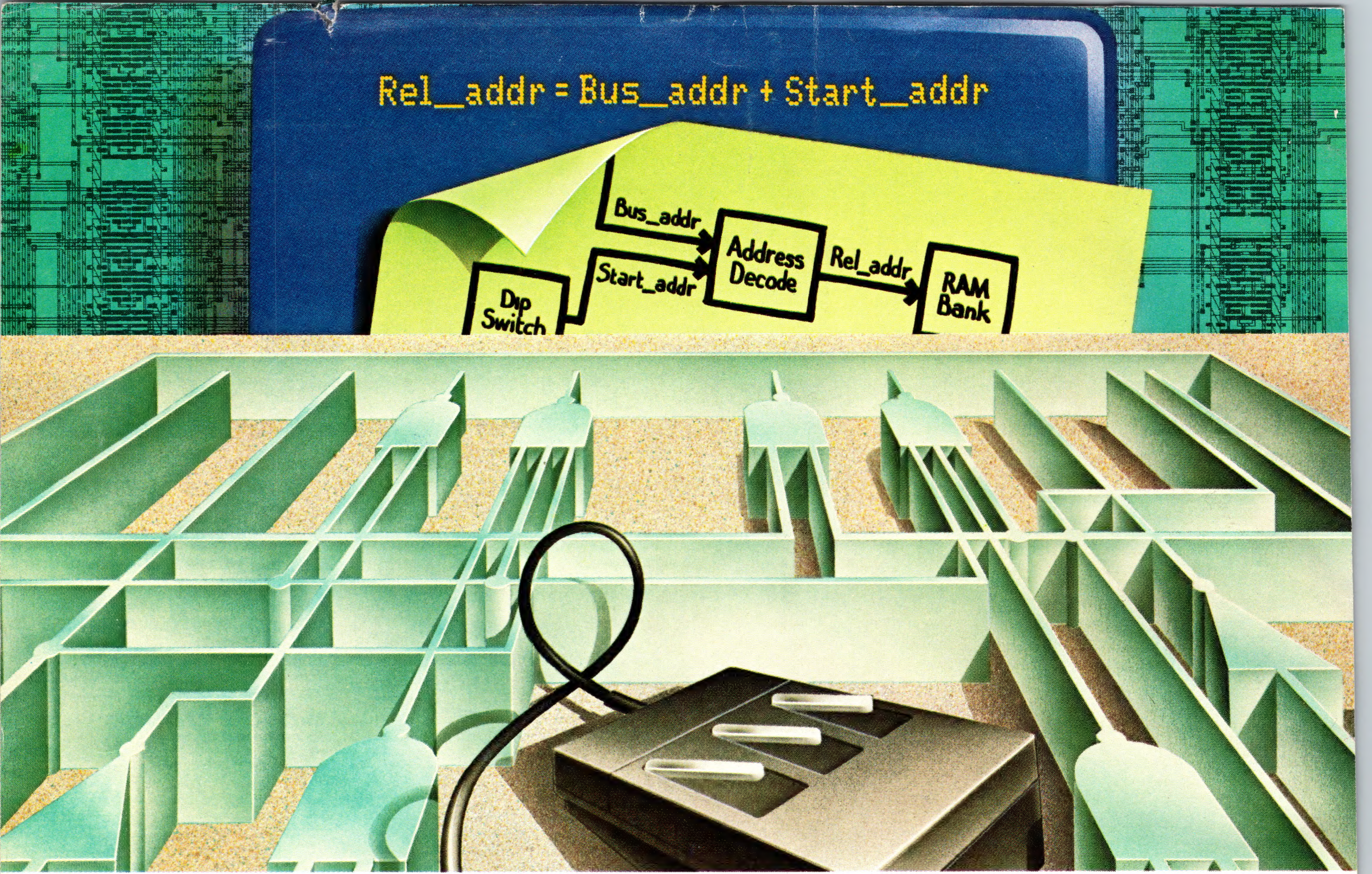

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